NTSC SYNC GENERATOR MODULE

Manual Number: A90-066341-04 TP Number: 06-076 Issue Number: 2

INTRODUCTION

The NTSC Sync Generator Module regenerates the incoming sync signal supplied by the sync separator stage on the Input Module.

Specific functions performed by the Sync Generator Module are listed below and discussed in the circuit description.

Video presence detection
Pulse generation from a 5 MHz clock
Horizontal phase adjustment
Vertical phase adjustment
Horizontal blanking timing adjustment
VIT line deletion selection (vertical blanking timing)
Burst flag timing adjustment

The Sync Generator Module produces all pulses necessary for the 3240 video processing amplifier, and for the accessory functions available as part of the processing amplifier system. It may also be used as the pulse generator in sync generator systems. Separated sync from input video or external reference is used to phase lock the Sync Generator Module.

CIRCUIT OVERVIEW Refer to schematic diagram E10-066341 sheets 1 and 2, and Figure 13 which is an overall block diagram.

Introduction

The Sync Generator Module is a phase-locked loop which may lock to sync separated from the external video (genlock mode) or subcarrier generated on the Color Lock Module (freerun mode).

Pulses produced by the Sync Generator IC are processed by the Timing Circuits to produce outputs which conform to the required width and timing constraints of the system. The Sync Generator IC is clocked by the 5 MHz VCO.

The H. Drive output of the Sync Generator is phase compared with the selected reference input, in the H Phase Detector. The H Phase Detector output is a dc voltage, the value of which corresponds to the measured phase difference; this voltage is applied through the 2-speed Loop Filter (an integrator) as a VCO control signal.

In the freerun mode (no video input) the Sync Generator Module locks to the H/2 signal, which is produced by dividing the Color Lock Module Subcarrier Output by 455.

Excessive time-base error will cause the Sync Generator to switch to fast loop filter operation, to enable the Sync Generator to follow the rapid changes in Sync phase. The UNLOCK indicator will light when the time-base error is too great for slow loop-speed operation. The FAST/ AUTO jumper may also be used to force the loop into the fast mode. This also forces the two-speed loop on the Color Lock Module into the fast mode. The UNLOCK indicator operates independently of the FAST/ AUTO switch.

Vertical phasing is provided by the Vertical Separator, which discriminates vertical sync by detecting six vertical serrations within a three and one-fourth lines period. The resulting reset pulse is delayed a number of lines by the Vertical Phase circuit, to bring the pulse into the same vertical phase as the input video.

Operating Modes and Adjustments

Default Modes

The generator will lock to input video containing a wide variety and severity of input signal impairments. However, if the time-base error or the input signal-to-noise ratio is excessive, it will automatically switch to one of the default modes described below.

No Video

If input video is not present, or if input noise is excessive, the video presence detector will not recognize vertical sync and will switch the sync generator to the freerun mode; i.e., it will frequency lock to the freerunning subcarrier oscillator on the Color Lock Module, and the NO VIDEO indicator will turn on. The Output Module will revert to color black or direct mode, depending on the position of the COLOR BLACK/DIRECT jumper S4 on the Sync Generator Module (Sheet 2 of Schematic, C/2).

Two-Speed Loop

If input time-base error is greater than approximately 1 microsecond within a one-field period, the Sync Generator will automatically switch to fast horizontal loop and follow the rapid changes in sync phase. The UNLOCK indicator will light when time-base error is excessive for the slow loop-speed condition. Loop speed also may be forced into the fast mode by the FAST/AUTO jumper, S1 (sheet 2, E/4). The UNLOCK indicator will operate independently of this switch function. This switch also will force the two-speed loop on the Color Lock Module into the fast mode.

Fine H Phase Adjustment

The fine H phase control, R71 (Sheet 1, E/4), has a range of approximately ± 150 ns. If more range is necessary, COARSE H PHASE programming jumpers are provided for adjusting horizontal phase in increments of 200 ns (Sheet 2, C/6). The jumpers program digital phase

information into the horizontal counters. As the number programmed in is incremented or decremented, the horizontal phase will delay or advance respectively. The number which gives the nominal horizontal phase is 0111. The vertical phase may be advanced one line by jumper S3 (Sheet 1).

H Blanking & Burst Flag

Each edge of horizontal blanking is adjustable independently (sheet 2, C/2 to D/2). The range of adjustment is >300 ns each edge. The leading edge adjustment is R91; the trailing edge is R93. Burst (flag) also has delay and width controls. They are each adjustable > 400 ns. The delay control is R98, and the width control is R100.

Freerunning SC/H Phase

When the video processor has no input video, the Sync Generator locks to subcarrier from the Color Lock Module. The phase relationship between the leading edge of sync and subcarrier in the Free Run mode is adjustable > ± 50 ns by R70 (Schematic, B/5, Sheet 1). The front-panel fine H phase control, R78, will have no effect.

Subcarrier Clocking

Subcarrier clocking causes the output sync to move in increments of 140 ns (1/2 SC cycle) if input sync phase drifts relative to subcarrier. This mode of operation will maintain the proper relationship of sync and subcarrier as established by the fine H phase control and the burst phase control. It is activated by S2 (sheet 1, D/5).

Vertical Blanking

Vertical blanking width is 20 or 21 lines, depending on the position of the #1 rocker on dip switch S6 (sheet 2, E/2). All other rockers on switches 5 and 6 are for unblanking whole lines on both fields from lines 10 - 20.

Vertical Phase

Vertical phase may be operated normally or advanced one line from input sync by using S3 (sheet 1, G/4).

Noise Window

The noise window serves two functions: (1) it increases noise immunity by rejecting all input pulses except those that occur approximately where sync is expected, and (2) it rejects the vertical component of sync. The width of the window is variable from 0.5 microsecond to 20 microseconds, depending on which of the WIDE WINDOW (window width select) jumpers (Sheet 2, B/7) are connected. Refer to Table 1. The window will go to the width selected by wide window jumpers when the horizontal phase-locked loop is acquiring lock, or if input time-base error is excessive. Under all other conditions, the window will be narrow. The narrow window may be defeated so that the generator always selects the wide window, by jumping the NARROW WINDOW turrets to 0 volts (sheet 1, E/7 - Window Width Select).

TABLE 1. WINDOW WIDTH SELECTION, WIDE WINDOW JUMPER

Position of Jumper	Window Width
1	20.0 microseconds
2	4.0 microseconds
3	2.0 microseconds
4	0.5 microsecond

CIRCUIT DESCRIPTION Refer to schematic E10-066341 (sheets 1 and 2) and Figure 13.

Horizontal Reference Preconditioning

Introduction

In the genlock mode, separated sync from input video or station sync (Ext Ref) is the reference frequency for the horizontal phase-locked loop, Figure 3. In the freerun mode, an internally-developed H/2 is the reference for the horizontal phase-locked loop. The separated sync is conditioned as follows before being sent to the horizontal phase detector (refer to Figure 1):

Noise windowing
Fine horizontal phase adjustment
Subcarrier clocking (optional)
An H/2 reference is provided in the absence of input video

Figure 2 shows the timing from the horizontal sync preconditioning section.

Noise Window (Schematic, E-F/7, sheet 1 and Figures 1 & 2)

Separated sync from the Input Module arrives through pin 24 of the rear connector. It is inverted by IC28(B) and is passed through data selector IC21. A leading edge pulse is then generated from this pulse by Q19. This narrow pulse is sent to the noise window, IC20(D) and IC29(B). The window is opened by a pulse arriving at pin 11 of IC29(B). The amount of time by which this pulse precedes the narrow pulse determines the width of the window. It will vary with the FINE H PHASE control.

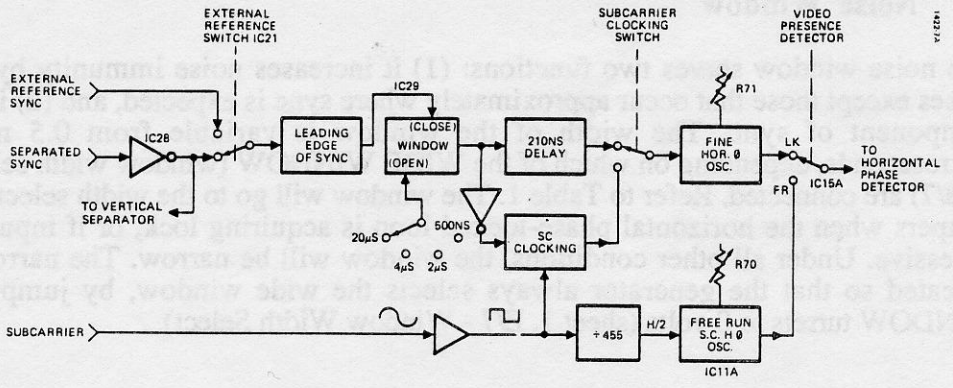


Figure 1. Horizontal Reference Preconditioning, Block Diagram

210 ns Delay (sheet 1)

The 210 ns delay compensates for the nominal delay of input sync through the subcarrier clocking circuit, so that noticeable changes in horizontal phase do not occur when switching from the clocking mode to the non-clocking mode.

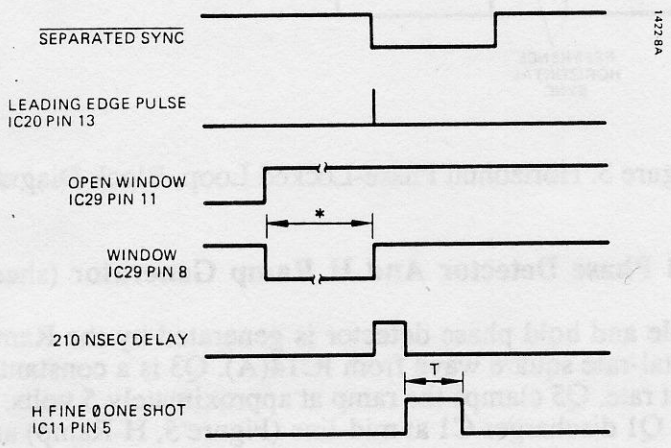


Figure 2. Horizontal Sync Preconditioning, Timing Diagram

Subcarrier Clocking (sheet 1)

In the subcarrier clocking mode, incoming horizontal sync is clocked with twice subcarrier frequency in IC45. IC46 is a voltage comparator which generates subcarrier square waves. IC36(A) and IC37(B) act as a frequency doubler. IC18 (B and C) form a digital switch which enables or disables the subcarrier clocking mode. It is activated by S2 (sheet 1, D/5). When processing monochrome video, the subcarrier clocking mode is disabled by the burst flag inhibit signal.

Fine H Phase & ÷ 455 Counter (sheet 1 and Figures 1 and 2)

IC11(A) is a highly stable one-shot multivibrator which is used for the fine horizontal phase adjustment. In the freerun mode, IC11(B) makes possible the adjustment of horizontal phase relative to subcarrier. The reference frequency for the horizontal PLL in the freerun mode is H/2 (7867 Hz). H/2 is generated by dividing down subcarrier with the ÷ 455 counter. IC15(A) selects the freerun or locked mode, depending on whether or not video is present.

Horizontal Phase-Locked Loop (sheet 2 and Figure 3)

The horizontal phase-locked loop includes two phase detectors operating in parallel to give the best performance of both. One is a sample and hold phase detector IC3, and the other is a phase coincidence detector IC4, IC5, & IC6. Figure 4 shows a block diagram of the horizontal phase detector, and Figure 5 shows the timing relationships for this section.

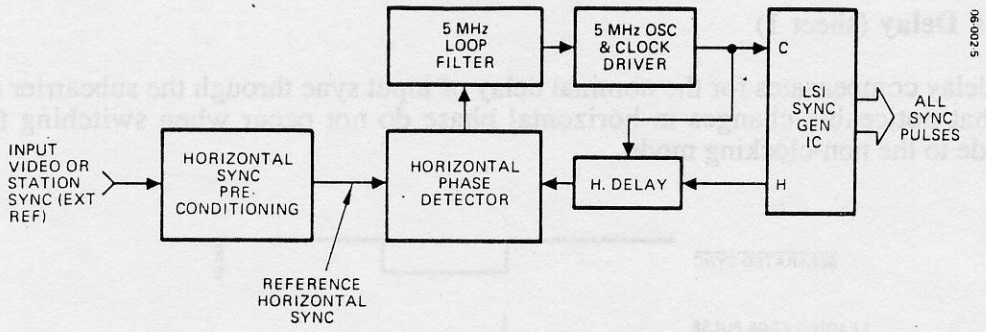


Figure 3. Horizontal Phase-Locked Loop, Block Diagram

Sample & Hold Phase Detector And H Ramp Generator (sheet 2)

The ramp for the sample and hold phase detector is generated by the Ramp Generator (sheet 2, G/7), using the horizontal-rate square wave from IC14(A). Q3 is a constant current source which charges C1 at a constant rate. Q5 clamps the ramp at approximately 5 volts. Q6 buffers the output of the Ramp Generator. Q1 discharges C1 at mid-line (Figure 5, H-Ramp) and holds it low for the duration of the line.

IC3, C3, Q7, and Q9 form the Sample and Hold. IC3 is an operational transconductance amplifier. Its output current is a function of the amplifier bias current applied to pin 5 and the differential voltage at input pins 2 and 3. When the current to pin 5 is zero and/or the input differential voltage is zero, there is no output current.

Q7 and Q9 form a unity-gain feedback pair with very high input impedance, and low output impedance. At the beginning of the sample period, Q8 (the sample pulse generator) turns off, and the amplifier bias current for IC3 is applied to pin 5 through resistor R13. The sample and hold circuit operates as a conventional voltage-mode op amp during the sample period. When the sample period ends, Q8 saturates and turns IC3 off. The hold capacitor, C3, retains the charge it had at the end of the sample.

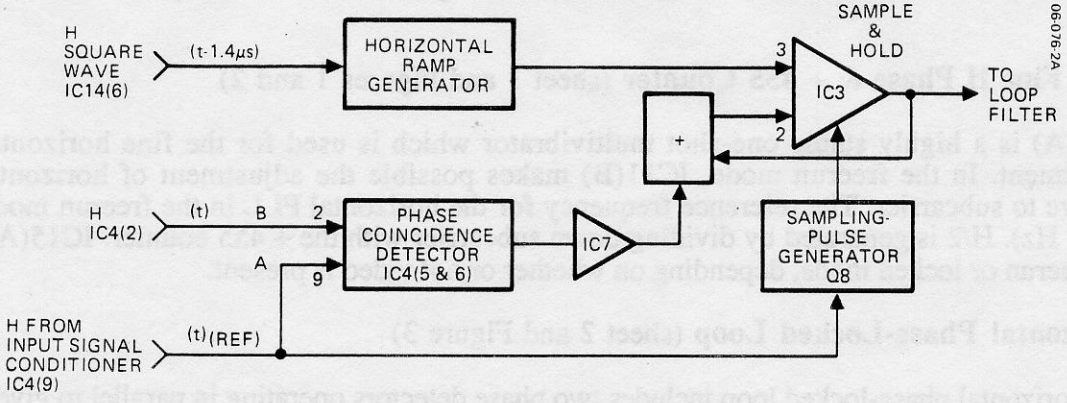


Figure 4. Horizontal Phase Detector, Block Diagram

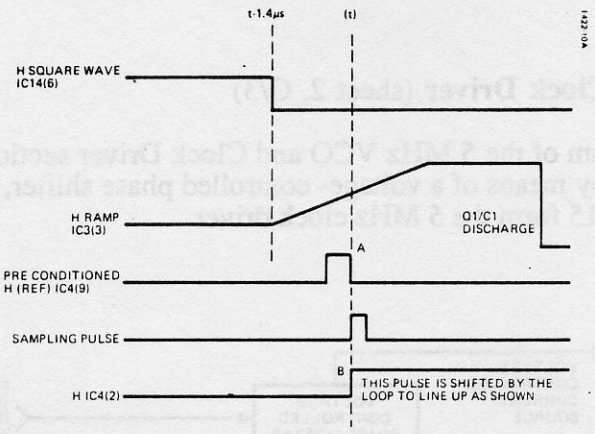


Figure 5. Horizontal Phase Detector, Timing Diagram

Phase Coincidence Detector (sheet 2, E/7)

The phase coincidence detector causes an offset of the sample in order to compensate for time and temperature variations. It achieves this by requiring that both trigger pulses to IC4 arrive at the same time. When both halves of IC4 are triggered, IC6 (A and B) will reset them. If both are triggered simultaneously, their output pulse widths will be equal and short. If one trigger leads the other, the one which leads will have the longer output pulse width up to the natural time out of the one-shot. This will result in a change of charge on integration capacitor C8. The resulting change in output voltage of IC7 will offset the sample and hold, and cause a coincidence of phase of the two trigger pulses (pulse marked "A" in Figures 4 and 5). IC5 is a memory which registers the occurrence of a trigger even after the one-shot times out. The memory is cleared at mid-line.

Loop Filter and Loss Of Lock Detector (sheet 2, G/4-5)

The circuit which includes IC2, R20-R22, and C6-C7, is the Loop Filter (Figure 6). The speed of the loop is selected by the FET switch, Q7. An out-of-lock or excessive time-base error condition is sensed by monitoring the sample-and-hold phase detector output voltage. Full wave peak detector D7 and D8 (Loss of Lock Detector) senses if the dynamic phase error has exceeded approximately 1 microsecond. If so, voltage comparator IC8(D)'s output will go positive. This will activate three conditions: (1) turn on loss of lock indicator D12, (2) activate the fast loop speed via D10, D1, and Q10, and (3) put the window into the WIDE mode. Switch S1 in FAST position activates the following: (1) forces loop into fast mode via IC6(D), IC8(C), and D9, (2) activates the wide window, and (3) forces the phase-locked loop on the Color Lock Module into fast mode.

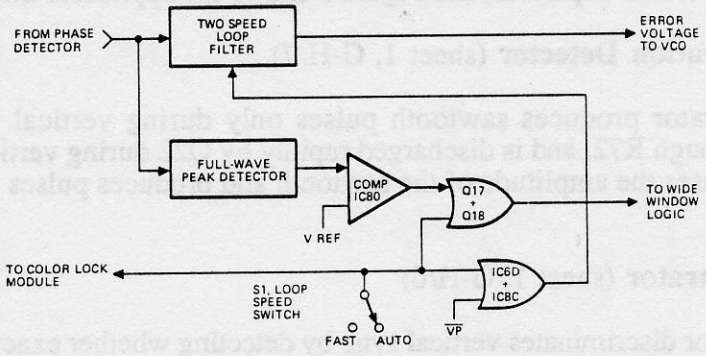


Figure 6. Two-Speed Loop Filter, Block Diagram

5 MHz VCO & Clock Driver (sheet 2, G/3)

Figure 7 is a block diagram of the 5 MHz VCO and Clock Driver section. The frequency of the 5 MHz VCO is controlled by means of a voltage- controlled phase shifter, IC1 (A and B), R26, R27, and C9. Transistors Q12-15 form the 5 MHz clock driver.

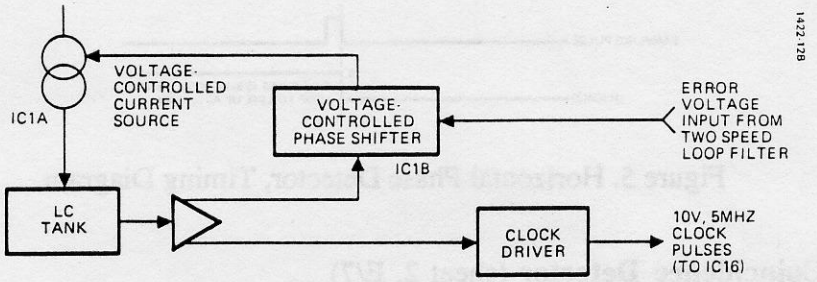


Figure 7. 5 MHz VCO and Clock Driver, Block Diagram

Sync Generator IC (sheet 2, C/5) IC16 is a CMOS LSI sync generator IC which provides timing signals for the Sync Generator Module. Some pulses are used just as they are (i.e., composite sync). Others have adjustable timing off-chip where required (i.e., composite blanking). The pulses which are used directly are buffered with IC17 and IC22 before being sent off the board.

Horizontal Delay Counter (sheet 2, C/6)

The horizontal delay counter (IC13 and surrounding circuitry) performs the following functions: (1) it delays horizontal timing to the phase detectors, which has the effect of causing the output pulses to advance from where they would otherwise be, and (2) by programming the delay, it provides horizontal phase adjustment in increments of 200 ns, and (3) it provides separate reference horizontal pulses to the phase detectors. The pulse to the sample and hold Ramp Generator leads the pulse sent to the phase coincidence detector by approximately 1.4 microseconds in order to start the ramp before the sample pulse. (See the Horizontal Phase Detector Timing Diagram, Figure 5).

Vertical Lock

Figure 8 shows the Vertical Separator, and Figure 9 shows the applicable timing relationships.

Vertical Serration Detector (sheet 1, G-H/7)

The sawtooth generator produces sawtooth pulses only during vertical sync. C27 is charged relatively slowly through R72, and is discharged rapidly by Q22 during vertical serrations. Voltage comparator IC32 senses the amplitude of the sawtooth and produces pulses during vertical sync.

Vertical Separator (sheet 1, G-H/6)

The Vertical Separator discriminates vertical sync by detecting whether exactly 6 vertical serrations occur within a 3-1/4-line period. Figure 9 shows the timing diagram for the Vertical Separator.

IC31(A) is a retriggerable one-shot. Its natural time-out pulse width is 3/4 of a line. It is triggered every 1/2 line by the leading edge of the 6 vertical pulses from the voltage comparator. It will time out 3/4 of a line after the last vertical pulse. During vertical sync, counter IC23(A) counts the trailing edge of the 6 vertical pulse. At the end of vertical sync, it should be in the "6" state. The 3/4 H one-shot will time out and deliver a reset pulse to the vertical pulse counter, the vertical reset generator, and the video presence detector. The width of the reset pulse is determined by the delay of R131 and C91. If, due to noise, the vertical pulse counter has counted more or less than 6, a vertical reset pulse will not be generated. The Sync Generator Module will then continue to lock to incoming horizontal sync until vertical sync is detected or until the Video Presence Detector causes it to freerun.

Vertical Reset Generator (sheet 1)

The sync generator IC (sheet 2) requires a vertical reset pulse which occurs a number of lines after vertical sync in order to have the same vertical phase as input video. This is accomplished by delaying the vertical reset pulse with the vertical phase counters. Switch S3 will allow one line of vertical phase advance if desired. IC15(B) disables the vertical reset pulse in the freerun mode.

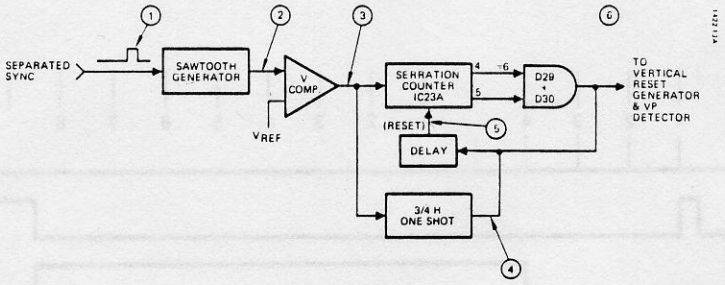


Figure 8. Vertical Separator, Block Diagram

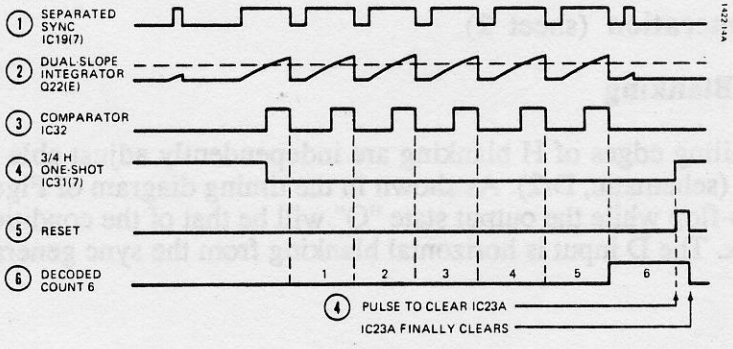


Figure 9. Vertical Separator, Timing Diagram

Video Presence Detector (sheet 1, F-G/4-5)

The Video Presence Detector must receive four consecutive vertical pulses in order to detect the presence of video, and approximately 8 fields of missing vertical pulses to indicate that video is not present. Figure 10 shows the timing diagram for the Video Presence Detector. IC31(B) is a retriggerable one-shot. Its timing is a function of the presence of video. When video is applied to the input, IC31(B) triggers on the first detected pulse from the vertical separator. Video presence has not yet been detected; therefore, the VP line is low, which turns Q26 on.

The delay of IC31(B) is then shortened to approximately 1-1/2 fields. If vertical sync is detected on consecutive fields, IC31(B) will be retriggered before it times out. IC23(B) will then count four fields and stop counting. If consecutive vertical fields are not detected, the one-shot will time out and reset counter IC23(B). The condition of the Q2 output of IC23(B) is the video presence indication. When video presence has been determined, the Q2 output will be high, turning off Q26. The one-shot time-out will then be lengthened to approximately 8 fields, which means there must be about 8 fields of video in which vertical sync is not detected before it will reset (IC23(B) and indicate the absence of video (NO VIDEO).

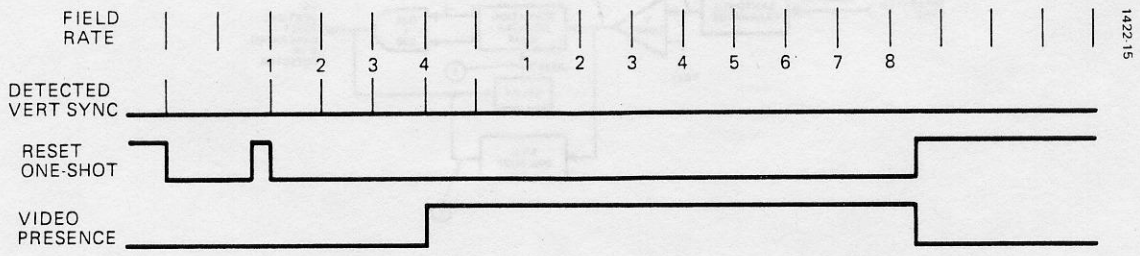


Figure 10. Video Presence Detector, Timing Diagram

Pulse Timing Generation (sheet 2)

Horizontal Blanking

The leading and trailing edges of H blanking are independently adjust able with a dual one-shot multivibrator, IC41 (schematic, D/2). As shown in the timing diagram of Figure 11, each one-shot will clock the D flip-flop while the output state "Q" will be that of the condition of the "D" input at the time of the clock. The D input is horizontal blanking from the sync generator IC, pin 37.

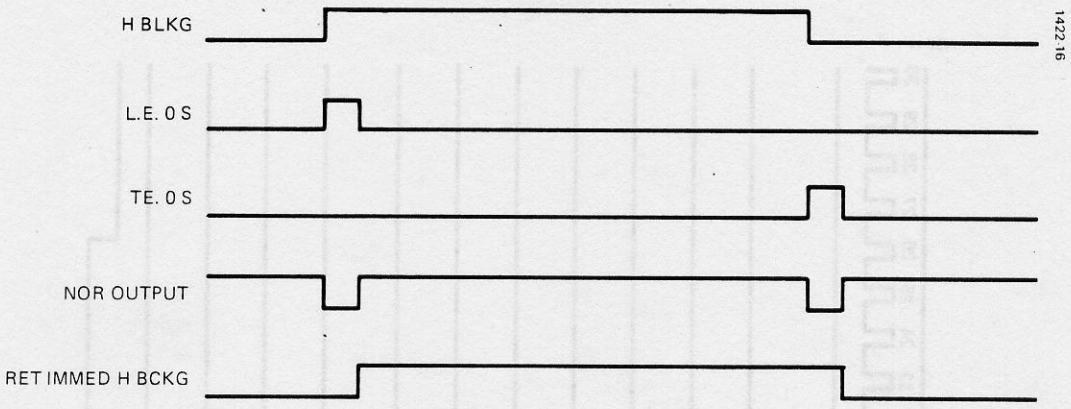


Figure 11. Horizontal Blanking, Timing Diagram

Horizontal Drive

Horizontal drive is gated with H blanking in IC27(A) so that the leading edge of H drive will be coincident with H blanking.

Vertical Blanking

Vertical blanking from the sync generator IC is gated with horizontal blanking in IC27(B) to produce composite blanking.

Toothed Blanking (E/2, sheet 2)

Toothed blanking is used in the blanking switch of the video processor Output Module. It allows vertical blanking of processed video to be defeated during any line from 10 - 21. Figure 12 shows the timing relationships. IC25 and IC40 are decoded Johnson (Mobius) counters. When clocked by horizontal drive, each output (Q1-Q8) sequentially produces a one-line-wide pulse. IC25 begins to count when reset by vertical drive. When it reaches the count of 9, it stops counting. This enables the clock to IC40, which counts to the count of 9 and holds. When an output is selected with dip switch S5 or S6, the pulse which occurs through that switch will inhibit vertical blanking during the line represented by the switch.

Line 21 vertical blanking inhibit is slightly different. It controls the vertical blanking width input of the sync generator IC. This will produce the correct vertical blanking width on even-numbered fields by allowing vertical blanking to end mid-line.

Burst Flag (Sheet 2, B/2)

Burst flag is derived from the leading edge of sync. IC42(A) triggers on sync but is inhibited during vertical blanking with $\overline{\text{VBLKG}}$ on pin 3. Burst enable is derived from the burst presence detector on the Color Lock Module so that burst is not produced when the Sync Generator Module is locked to monochrome video.

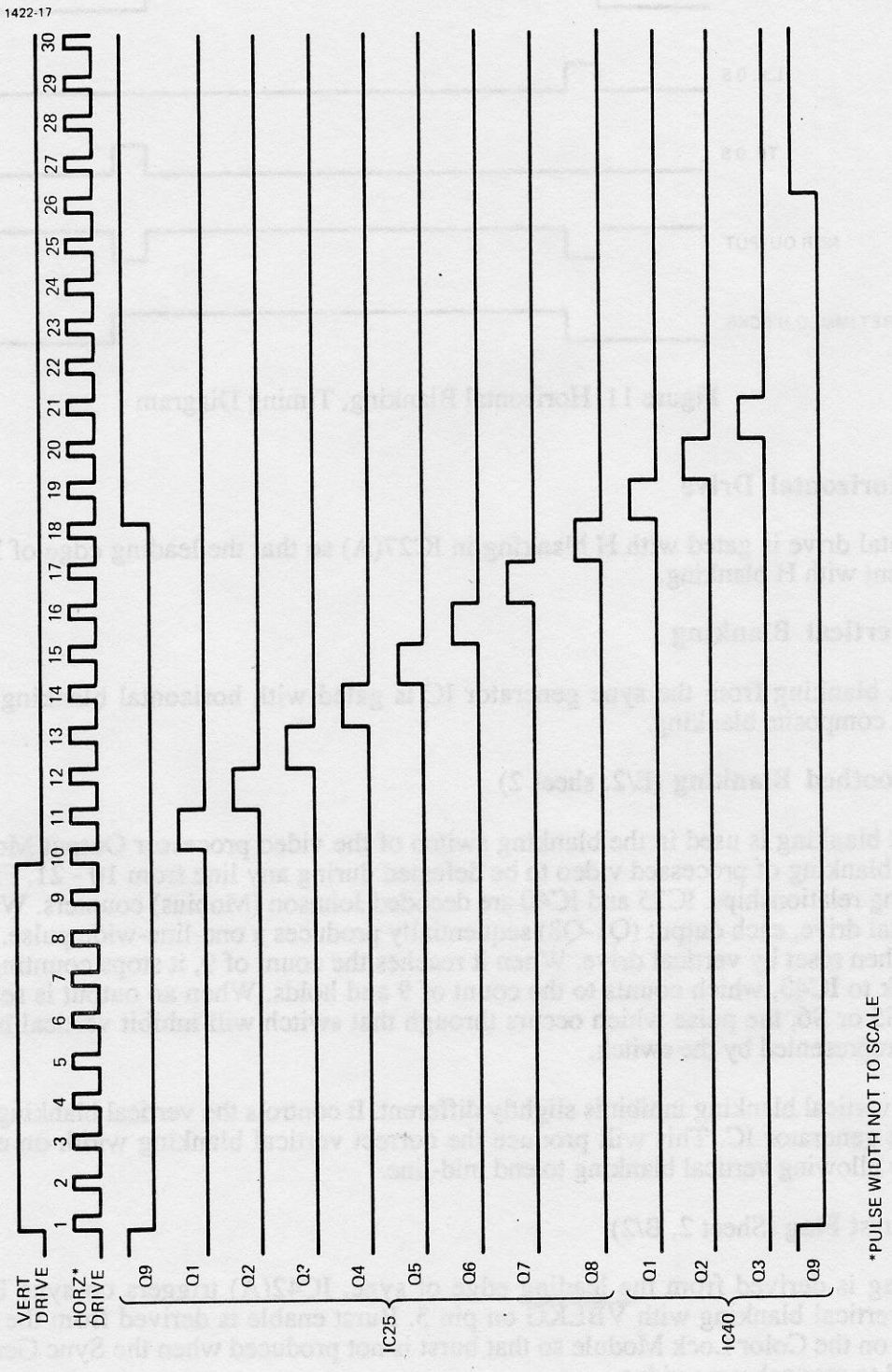


Figure 12. Toothed Blanking, Timing Diagram

5V Power Supply Refer to Sheet 1 of the schematic diagram.

The 5-volt supply is chopper regulated. The drive pulses for pass transistor Q550 are derived from 2H (31.5 kHz) from the sync generator IC. The 10-volt 2H pulses are divided by R567 and R568 to about 3 volts, then buffered by Q551. Q554 is a switch which drives a one-shot multivibrator, Q553. The duty cycle of the pulses produced by Q553 determine the ratio of voltage drop from the 15-volt supply. This duty cycle is affected by the following conditions:

R558 is connected to the 15-volt supply and therefore causes feedforward voltage regulation by changing the pulse width of the one-shot. R558 serves primarily to improve transient response.

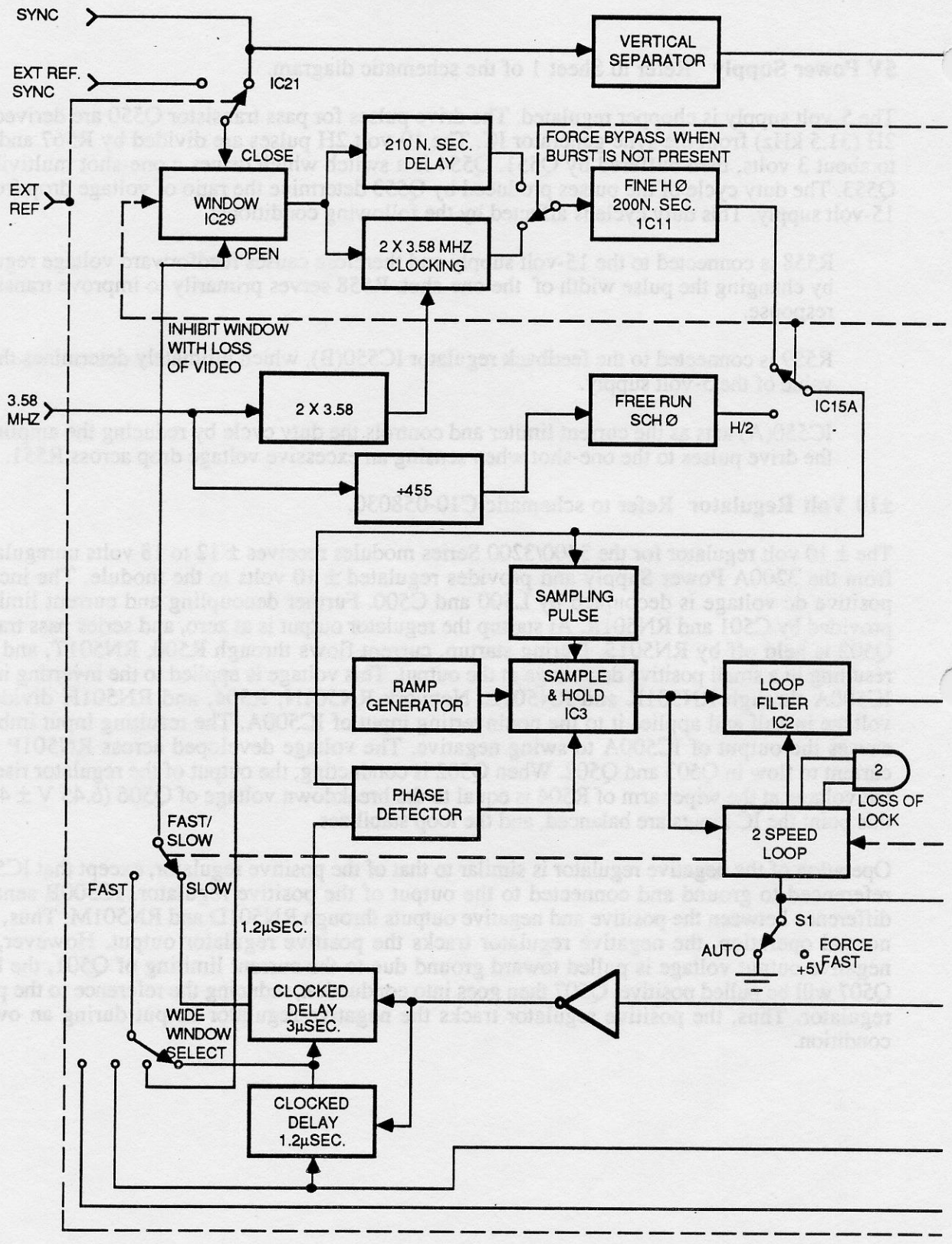
R559 is connected to the feedback regulator IC550(B), which ultimately determines the final value of the 5-volt supply.

IC550(A) acts as the current limiter and controls the duty cycle by reducing the amplitude of the drive pulses to the one-shot when sensing an excessive voltage drop across R551.

±10 Volt Regulator Refer to schematic C10-058030.

The ± 10 volt regulator for the 3400/3200 Series modules receives ± 12 to 18 volts unregulated dc from the 3200A Power Supply and provides regulated ± 10 volts to the module. The incoming positive dc voltage is decoupled by L500 and C500. Further decoupling and current limiting is provided by C501 and RN501R. At startup the regulator output is at zero, and series pass transistor Q502 is held off by RN501S. During startup, current flows through R500, RN501T, and R502, resulting in a small positive dc voltage at the output. This voltage is applied to the inverting input of IC500A through RN501K and RN501L. Network RN501N, R504, and RN501H divides this voltage in half and applies it to the noninverting input of IC500A. The resulting input imbalance causes the output of IC500A to swing negative. The voltage developed across RN501P causes current to flow in Q503 and Q502. When Q502 is conducting, the output of the regulator rises until the voltage at the wiper arm of R504 is equal to the breakdown voltage of Q506 (6.45 V ± 4%). At this point the IC inputs are balanced, and the loop stabilizes.

Operation of the negative regulator is similar to that of the positive regulator, except that IC500B is referenced to ground and connected to the output of the positive regulator. IC500B senses the difference between the positive and negative outputs through RN501D and RN501M. Thus, during normal operation, the negative regulator tracks the positive regulator output. However, if the negative output voltage is pulled toward ground due to the current limiting of Q501, the base of Q507 will be pulled positive. Q507 then goes into conduction, reducing the reference to the positive regulator. Thus, the positive regulator tracks the negative regulator output during an overload condition.


SYNC
EXT REF. SYNC
IC21
VERTICAL SEPARATOR
CLOSE
210 N. SEC. DELAY
FORCE BYPASS WHEN BURST IS NOT PRESENT
EXT REF
WINDOW IC29
FINE H Ø 200N. SEC. 1C11
OPEN
2 X 3.58 MHZ CLOCKING
INHIBIT WINDOW WITH LOSS OF VIDEO
3.58 MHZ
2 X 3.58
FREE RUN SCH Ø
H/2
IC15A
+455
SAMPLING PULSE
RAMP GENERATOR
SAMPLE & HOLD IC3
LOOP FILTER IC2
2
LOSS OF LOCK
PHASE DETECTOR
FAST/ SLOW
2 SPEED LOOP
FAST
SLOW
1.2µSEC.
S1
AUTO
FORCE +5V FAST
CLOCKED DELAY 3µSEC.
WIDE WINDOW SELECT
CLOCKED DELAY 1.2µSEC.

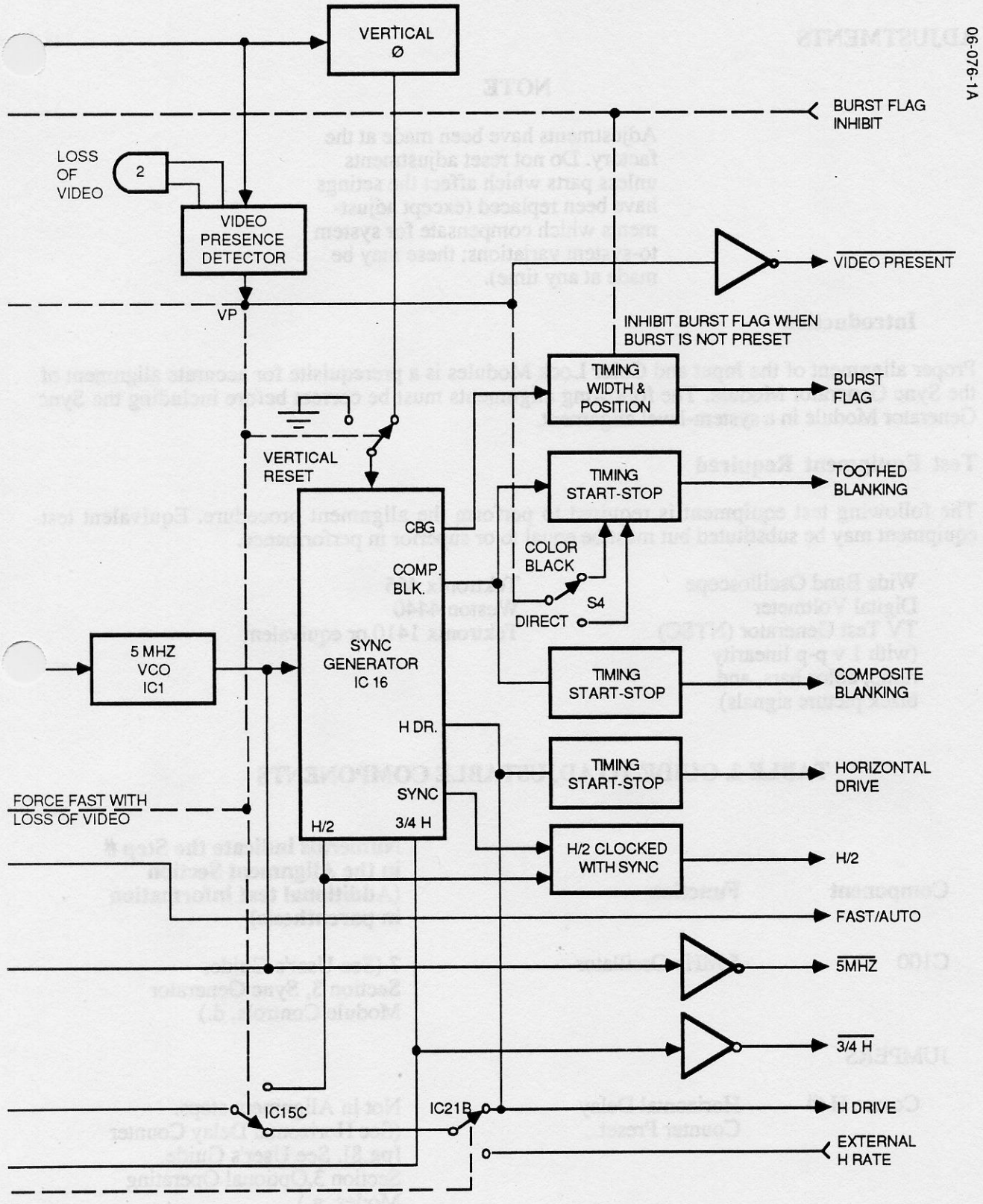


Figure 13. Function Diagram, NTSC Sync Generator Module

ADJUSTMENTS

NOTE

Adjustments have been made at the factory. Do not reset adjustments unless parts which affect the setings have been replaced (except adjustments which compensate for system to-system variations; these may be made at any time).

Introduction

Proper alignment of the Input and Color Lock Modules is a prerequisite for accurate alignment of the Sync Generator Module. The following alignments must be correct before including the Sync Generator Module in a system-level alignment.

Test Equipment Required

The following test equipment is required to perform the alignment procedure. Equivalent test equipment may be substituted but must be equal to or superior in performance.

Wide Band Oscilloscope	Tektronix 465
Digital Voltmeter	Weston 4440
TV Test Generator (NTSC) (with 1 v p-p linearity ramp, color bars, and black picture signals)	Tektronix 1410 or equivalent

TABLE 2. GUIDE TO ADJUSTABLE COMPONENTS

Component	Function	Numerals indicate the Step # in the Alignment Section (Additional text information in parenthesis)
C100	5 MHz Oscillator	7 (See User's Guide, Section 3, Sync Generator Module Controls, d.)
JUMPERS		
Coarse H Ø	Horizontal Delay Counter Preset	Not in Alignment steps. (See Horizontal Delay Counter [pg.8]. See User's Guide, Section 3,Optional Operating Modes, g.)

TABLE 2. GUIDE TO ADJUSTABLE COMPONENTS (cont.)

Component	Function	Numerals indicate the Step # in the Alignment Section (Additional text information in parenthesis)
JUMPERS (Continued)		
40/60	Set for use with 3240 or 3260 System	5 (schematic, Sheet 2, A-B/ 6-7)
Narrow Window (Defeat)	Forces user selected WIDE WINDOW to always be in effect	5 (See Noise Window [pg.4] See Schematic, Sheet 1, E/7. See User's Guide, Section 3, Optional Operating Modes, k.)
Wide Window (Defeat)	Determines the widest width of the noise window (used only during unlocked conditions.)	
POTENTIOMETERS		
R5	Ramp Generator current	8
R70	SC/H Phase in free-run mode	See Service Manual, Section 5 SC/H Phasing (pg.5-6).
R71	Fine H Phase	10 (See Fine H Phase [pg.2]. See User's Guide, Section 3, Sync Generator Module Controls, a.).
R91,93	Horizontal Blanking position/width	11
R98,100	Burst Flag position/width	12
R504	±10V Regulators	1

TABLE 2. GUIDE TO ADJUSTABLE COMPONENTS (cont.)

Component	Function	Numerals indicate the Step # in the Alignment Section (Addtional text information in parenthesis)
Switches		
S1	Horizontal and Colorlock Loop-Speeds	4 (See Loop Filter and Loss of Lock Detector [pg.7]. Also see in Circuit Overview's, Introduction [pg.1 & 2], Operating Modes and Adjustments: Default Modes, Two- Speed Loop [pg.2]. See User's Guide Section 3, Optional Operating Modes, f.)
S2	Subcarrier Clocking	4 (See Circuit Overview, Subcarrier Clocking. See Circuit Description, Subcarrier Clocking. See Service Manual, Section 5, SC/H Phasing after step 6.)
S3	Vertical Phase Line Advance	4 (See Vertical Lock [pg.8], Vertical Reset Generator [pg.9]. See User's Guide, Optional Operating Modes, h.)
S4	Direct/Color Black Default	4 (See Default Modes and No Video [pg.2].)
S5,6	Vertical Toothed Blanking Switches	Not in Alignment steps. (See Figure 12 and text on Toothed Blanking [pg.11]. See User's Guide, Section 3, Optional Operating Modes, j.)

Alignment Procedure

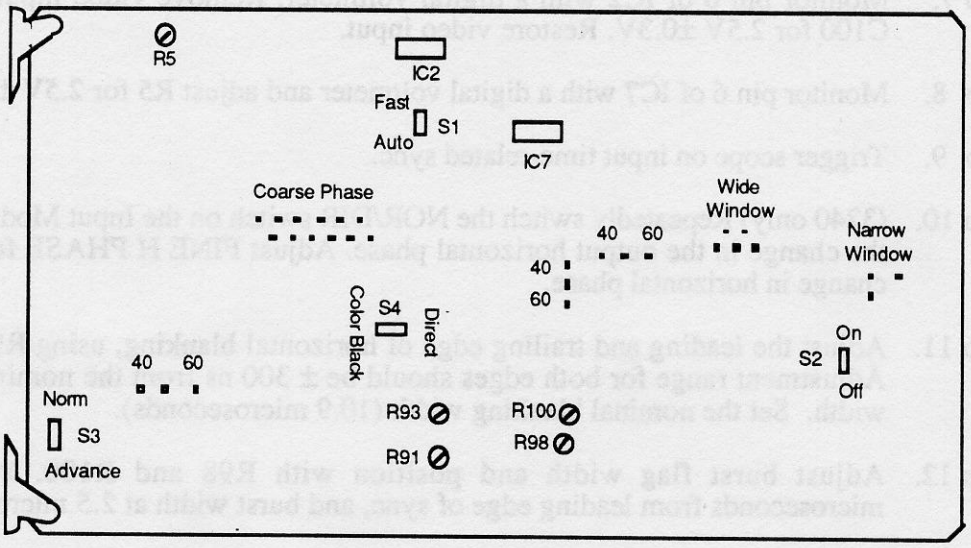


Figure 14. 3240 NTSC Sync Generator Component Location

Step 1. After applying power, connect a digital voltmeter to the +10 volt test point. Adjust trimpot R501, REG SET, to +10 volts.

Step 2. Check the -10 volt test point. It should be -10 V ± 0.05 V.

Step 3. Check the +5 volt power supply at the cathode end of D554. The reading should be +5 volts, ± 50 mV.

Step 4. Set the jumpers to the following positions:

S1 - FAST
S2 - OFF
S3 - NORM
S4 - COLOR BLACK

Step 5. Place the jumpers as follows:

NARROW WINDOW	Strap parallel to rear connector (not to ground)
WIDE WINDOW	Strap to #3 (on 3260 systems, strap to #4)
COARSE PHASE	Select 0111
40/60 TURRETS	Select 40 on 3240 Systems or 60 on 3260 Systems.

Step 6. Connect input video to the system frame. The input video should conform to RS170A standards.

Step 7. Monitor pin 6 of IC2 with a digital voltmeter. Remove video input and adjust C100 for 2.5V ±0.3V. Restore video input.

Step 8. Monitor pin 6 of IC7 with a digital voltmeter and adjust R5 for 2.5V ±0.3V.

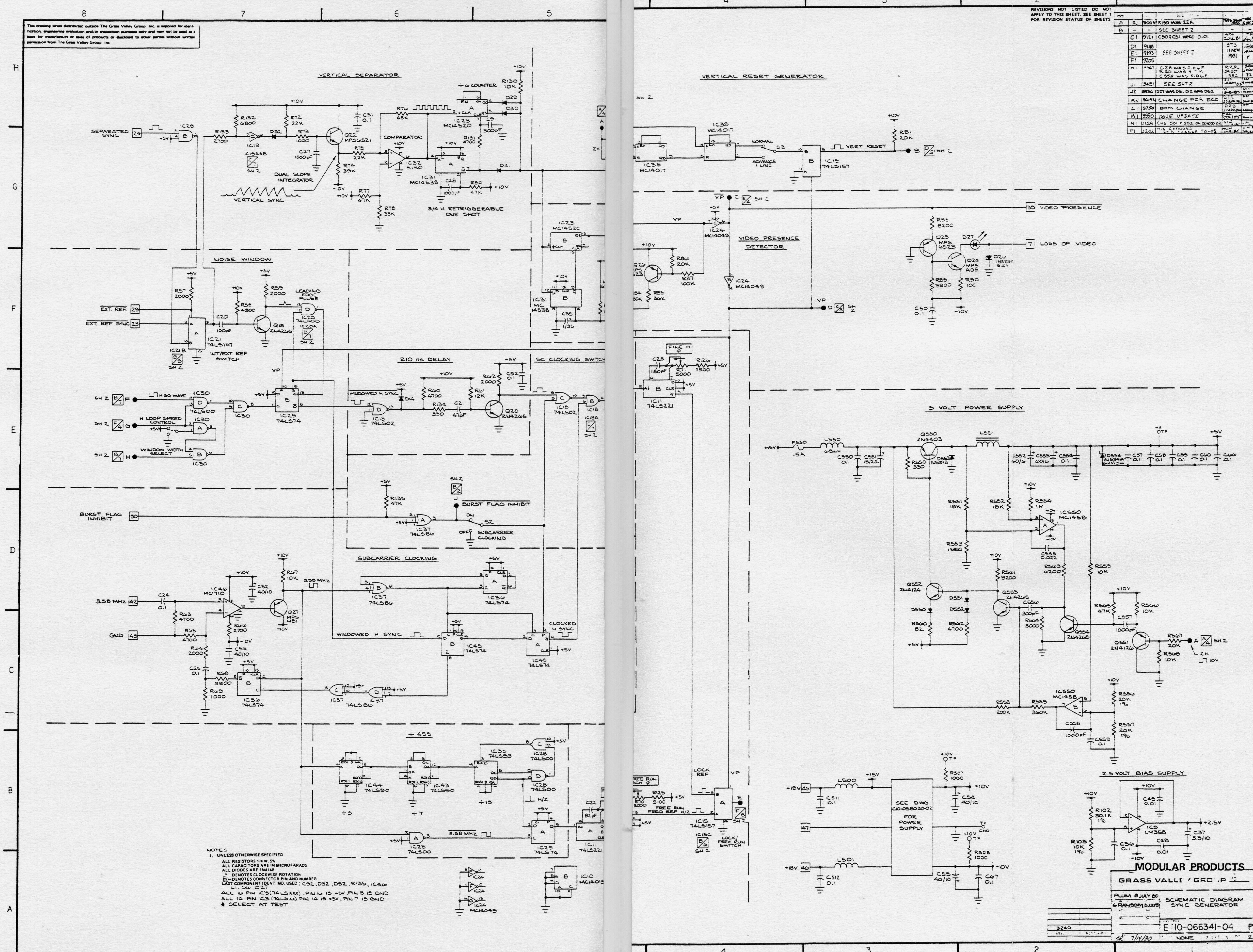
Step 9. Trigger scope on input time-related sync.

Step 10. (3240 only) Repeatedly switch the NOR/DIR switch on the Input Module and note the change in the output horizontal phase. Adjust FINE H PHASE for minimum change in horizontal phase.

Step 11. Adjust the leading and trailing edge of horizontal blanking, using R91 and R93. Adjustment range for both edges should be ± 300 ns from the nominal blanking width. Set the nominal blanking width (10.9 microseconds).

Step 12. Adjust burst flag width and position with R98 and R100. Position 5.3 microseconds from leading edge of sync, and burst width at 2.5 microseconds.

Step 13. (3240 only) Remove the input video. Note if color black appears at the output. Switch S4 to DIRECT position. Color black should disappear. Return switch S4 to COLOR BLACK position.



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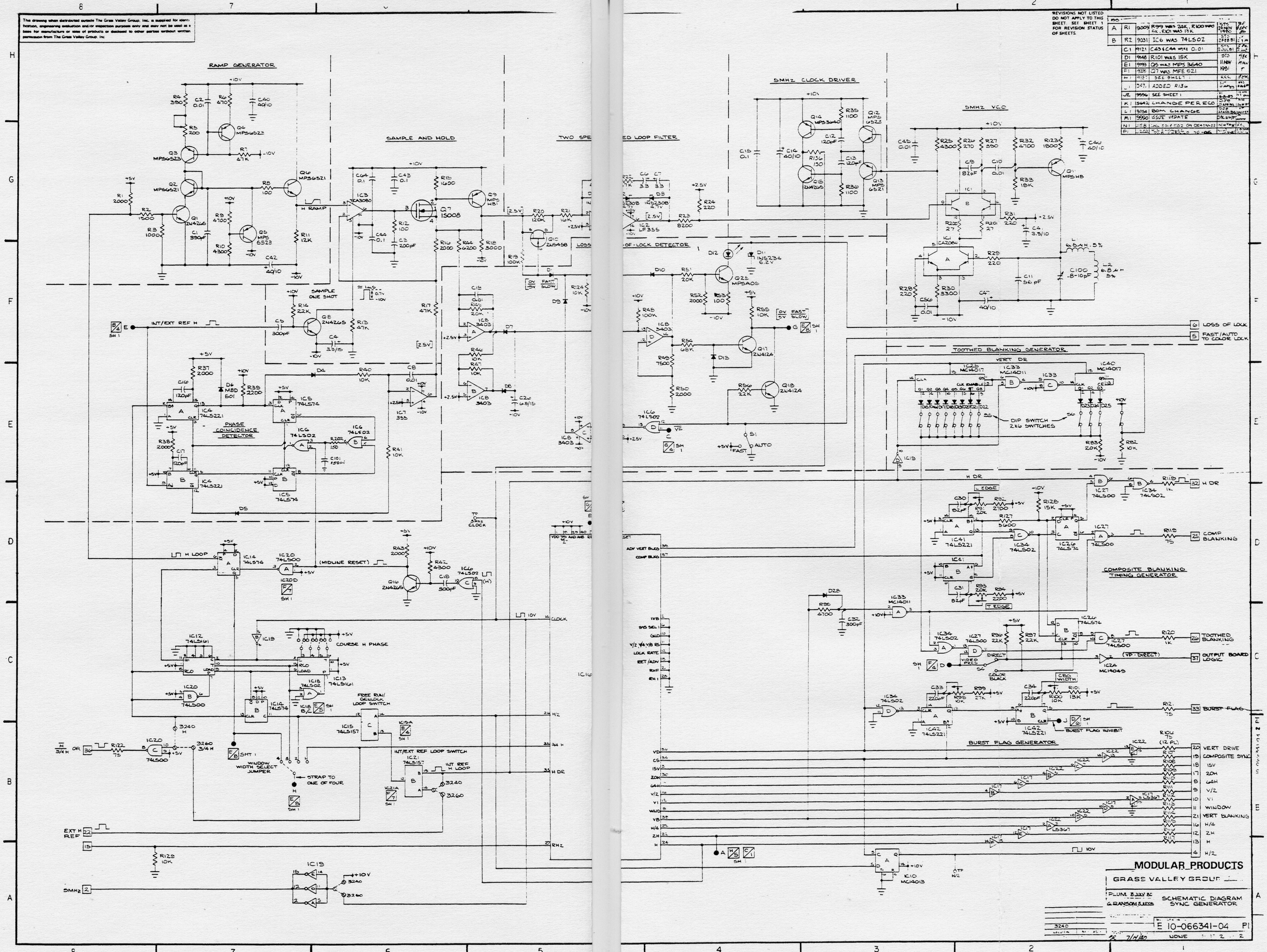
VERTICAL SEPARATOR
SEPARATED SYNC
DUAL SLOPE INTEGRATOR
VERTICAL SYNC
COMPARATOR
÷6 COUNTER
3/4 H RETRIGGERABLE ONE SHOT
NOISE WINDOW
EXT REF
EXT. REF SYNC
INT/EXT REF SWITCH
LEADING EDGE PULSE
H SQ WAVE
H LOOP SPEED CONTROL
WINDOW WIDTH SELECT
210 ns DELAY
WINDOWED H SYNC
SC CLOCKING SWITCH
BURST FLAG INHIBIT
SUBCARRIER CLOCKING
3.58 MHz
GND
CLOCKED H SYNC
÷455
÷5
÷7
÷13
VERTICAL RESET GENERATOR
NORMAL
ADVANCE 1 LINE
VERT RESET
VIDEO PRESENCE
VIDEO PRESENCE DETECTOR
LOSS OF VIDEO
FINE H
LOCK REF
FREE RUN
FREE REF H/2
LOCK/FREE RUN SWITCH
5 VOLT POWER SUPPLY
SEE DWG 010-058030-02 FOR POWER SUPPLY
2.5 VOLT BIAS SUPPLY
NOTES:
1. UNLESS OTHERWISE SPECIFIED
ALL RESISTORS 1/4 W, 5%
ALL CAPACITORS ARE IN MICROFARADS
ALL DIODES ARE 1N4148
DENOTES CLOCKWISE ROTATION
DENOTES CONNECTOR PIN AND NUMBER
LAST COMPONENT IDENT. NO. USED: C92, D32, D52, R135, IC46, L1, S6, Q27
ALL 16 PIN IC'S (74LSXXX), PIN 16 IS +5V, PIN 8 IS GND
ALL 14 PIN IC'S (74LSXX) PIN 14 IS +5V, PIN 7 IS GND
* SELECT AT TEST
REVISIONS NOT LISTED DO NOT APPLY TO THIS SHEET. SEE SHEET 1 FOR REVISION STATUS OF SHEETS
R130 WAS 22K
SEE SHEET 2
C50 & C51 WERE 0.01
SEE SHEET 2
SEE SHT 2
CHANGE PER ECO
BOM CHANGE
ISSUE UPDATE
MODULAR PRODUCTS
GRASS VALLEY GROUP
PLUM 8 JULY 80
G RANSOM 8 JULY 80
SCHEMATIC DIAGRAM SYNC GENERATOR
E 10-066341-04
3240
7/14/80
NONE
2



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REVISIONS NOT LISTED DO NOT APPLY TO THIS SHEET. SEE SHEET 1 FOR REVISION STATUS OF SHEETS.
A R1 9009 R99 WAS 24K, R100 WAS 5K, R101 WAS 13K STS 24 NOV 1980
B R2 9031 IC6 WAS 74LS02 STS 2 FEB 81
C1 9121 C43 & C44 WERE 0.01 STS 2 JUL 81
D1 9148 R101 WAS 15K STS 11 NOV 1981
E1 9193 Q5 WAS MPS 3640
F1 9205 Q7 WAS MFE 521
SEE SHEET 1
ADDED R136
J2 9556 SEE SHEET 1
K1 9642 CHANGE PER ECO
L1 9754 BOM CHANGE
M1 9990 ISSUE UPDATE
RAMP GENERATOR
SAMPLE AND HOLD
SAMPLE ONE SHOT
PHASE COINCIDENCE DETECTOR
5MHz CLOCK DRIVER
5MHz VCO
LOSS-OF-LOCK DETECTOR
TOOTHED BLANKING GENERATOR
DIP SWITCH 2x6 SWITCHES
COMPOSITE BLANKING TIMING GENERATOR
BURST FLAG GENERATOR
COURSE H PHASE
FREE RUN/GENLOCK LOOP SWITCH
INT/EXT REF LOOP SWITCH
WINDOW WIDTH SELECT JUMPER
STRAP TO ONE OF FOUR
(MIDLINE RESET)
INT/EXT REF H
H LOOP
H RAMP
LOSS OF LOCK
FAST/AUTO TO COLOR LOCK
H DR
COMP BLANKING
TOOTHED BLANKING
OUTPUT BOARD LOGIC
BURST FLAG
BURST FLAG INHIBIT
VERT DRIVE
COMPOSITE SYNC
15V
20H
64H
V/2
V1
WINDOW
VERT BLANKING
H/4
2H
H
H/2
EXT H REF
5MHz
MODULAR PRODUCTS
GRASS VALLEY GROUP
PLUM 8 JULY 80
G. RANSOM 8 JULY 80
SCHEMATIC DIAGRAM
SYNC GENERATOR
3240
E 10-066341-04 P1
7/14/80
NONE
2 2