EXTERNAL REFERENCE MODULE

Manual Number: A90-066343-02/12 TP Number: 06-044 Issue Number: 2

INTRODUCTION

The External Reference Module is an option for the 3240-series Video Processor Systems. The module allows the sync and subcarrier regeneration circuits of the processor to be locked to externally applied sync and subcarrier. The -02 version of the External Reference Module is for NTSC operation; the -12 version is for PAL. Differences between the versions involve circuit changes which are noted on the module schematic diagram.

SPECIFICATIONS

Specifications for the External Reference Module are listed in Table 1.

TABLE 1. EXTERNAL REFERENCE SPECIFICATIONS

Temperature range:	
For specifications	0 to 50 degrees C
Inputs:	
Sync	Loop-through, 1 to 8 volts, single-ended, 40 dB return loss at 5 MHz
Subcarrier	Loop-through, 0.5 volt to 4 volt, single-ended, 40 dB return loss at 5 MHz
Time base error	10 nanoseconds total
External sync timing	-.5, +1.5 microseconds relative to input video
Subcarrier phase range	360 degrees, 60 degree step, 90 degrees continuous
Nonsynchronous capability	Auto/forced internal/forced external

TABLE 1. EXTERNAL REFERENCE SPECIFICATIONS (continued)

Inputs:	
Attack time	>8 lines (approximately)
Release time	>1 frame, <2 frames (approximately)
Windows:	
Horizontal	± 100 nanoseconds to ± 500 nanoseconds, ± 400 nanoseconds std.
Vertical	<1/2 line
Subcarrier	± 15 degrees std., ± 10 degrees min, ± 40 degrees maximum
Input power	4 watts maximum

INSTALLATION

NOTE
(NTSC versions)

To earlier versions of the video processor, modifications may be necessary to accomodate the External Reference Module. Contact Grass Valley Group Customer Service for Field Modification Note 1048 and further instructions, if:

A. On the Color Lock Module (assembly number 066339), the dash number following the assembly number is lower than -01, or:

B. On the Sync Generator Module (assembly number 066341), the dash number following the assembly number is lower than -03, or:

C. On the processor frame (assembly number 093683), the dash number following the assembly number is lower than -01.

(On circuit modules the assembly number is located near the title, and the dash number is hand-lettered on. On frames the assembly number is located on an adhesive label located inside one of the power supply module cells.)

Remote Connections

Remote connections include the external reference mode switch, S2, and the external reference indicator LED. GVG's remote panel is prewired to control the External Reference option. When the module is to be operated by remote control, mode switch S2 should be left in the "AUTO", or center position.

For custom panel designs, the following guidelines may be helpful:

MODE SELECT - Mode select is accomplished by connecting one of two mode select leads to ground or leaving both leads open. Refer to 26-pin connector J30 at the rear of the processor tray.

For external reference, ground J30, pin 20 (leave pin 22 open).

For internal reference, ground J30, pin 22 (leave pin 20 open).

For automatic selection, leave pins 20 and 22 of J30 open-circuited.

For a remote LED mode indication, connect the remote LED cathode to J30, pin 21, and the anode to ground. The output is a current source, so no limiting resistor is necessary.

Two LEDs may be connected in series. A voltage-reference zener can be installed in series with an LED to provide a fail-safe connection.

For a high TTL logic level at pin 25 corresponding to the no-sync output of the nonsynchronous detector, the jumper between terminals J and H, on the External Reference Module, must be removed. For a low TTL logic level output corresponding to no sync a jumper must be installed between terminals J and H.

Initial Set-Up

1. Insert the following modules into the video processor frame:

   Input Module
   Output Module
   Color Lock Module
   Sync Generator Module

2. Apply a reference video input to the processor without the External Reference Module, and make initial adjustments as per the system instruction manual. Turn off the subcarrier clocking switch on the Sync Generator Module.

3. Insert the External Reference Module.

4. Connect external sync and subcarrier signals to the processor frame at J12 and J14.

5. Terminate J13 and J15 with 75 ohms.

Horizontal Phase Installation Adjustments

6. Trigger an oscilloscope with external sync. Set S2 on the External Reference Module to INT. Observe the video output on the oscilloscope and note the position of the sync leading edge.

7. Set S2 to EXT. Adjust R63 to bring the video output sync leading edge to the position observed in Step 6. This makes external sync timing coincident with video sync timing.

8. Observe the waveform at TP2 and adjust R64 for minimum pulse width. This centers the horizontal non-synchrones detector in its window.

Subcarrier Phase Installation Adjustments

NOTE

For this adjustment, the jumper between pins S and T must be removed.

9. Connect the external subcarrier to the reference input of a vectorscope. Observe burst phase of the subcarrier output on the vectorscope. Turn S2 to INT. Adjust the vectorscope to place subcarrier phase at 0 degrees. Turn S2 to EXT. Adjust the step and fine phase controls of the External Reference Module to move subcarrier phase back to 0 degrees.

10. Turn S2 to AUTO. All LEDs should be off (except for EXT REF DS5), and the processor should be locked to external sync and subcarrier.

NOTE
(NTSC ONLY)

If the SC CLOCKING switch on the Sync Generator Module is set to ON position, the video output sync may jump in 140 nanosecond steps while the external subcarrier phase is being adjusted.

11. Observe burst phase of the video output on the vectorscope. Turn S2 to INT. Adjust the vectorscope to have burst phase at 0 degrees. Turn S2 to EXT. Adjust C54 to move burst phase back to 0 degrees.

OPERATION

Controls and Indicators

Potentiometer R63 adjusts the H phase of the external sync.

Potentiometer R64 adjusts the centering of the horizontal synchronous detector.

S1, STEP Ø adjustment (operates in conjunction with R151)
S2, Switch Positions: (S2 can be remotely positioned)
A - Internal lock
B - Auto (position for remote control operation)
C - External lock

R151, FINE Ø adjustment (operates with S1 for 360 degree range)

TABLE 2. INDICATOR FUNCTIONS

LED (Front of Module)	When lighted Indicates Indicates	When Off
DS1	Vertical nonsynchronous	Vertical synchronous
DS2	H nonsynchronous	H synchronous
DS3	Subcarrier phase out of lock range	Subcarrier within lock range
DS4	Video not present	Video present
DS5*	Internally locked	Externally locked

*DS5 can be remotely positioned. DS5 indication can be reversed by removing the jumper on turrets K and L.

Operating Mode Selections

1. If, in the external reference mode, the processor is to insert external sync on the output signal, along with regenerated burst which is phase-locked to incoming burst:

   a. Remove jumper from turrets Q and R.
   b. Place a jumper between the +5 volt test point and TP7.

2. If the subcarrier nonsynchronous input is to be disregarded in he automatic logic, remove jumper between A and B.

3. If the horizontal nonsynchronous input is to be disregarded in the automatic logic, remove jumper between C and D.

4. If the vertical nonsynchronous input is to be disregarded in the automatic logic, remove jumper between E and F.

5. If internally generated burst is always to appear on the output video, regardless of whether burst is present on the input video,

   a. Place a jumper between S and T.
   b. Remove jumper from turrets A and B.

6. Subcarrier phase synchronous window phase adjustment resistor R150 is mounted on turrets. Its value determines the subcarrier phase synchronous window. It is shipped with R150 equal to 10K ohm, for a window of approximately ± 15 degrees. Table 3 can be used as a selection guide for modification:

TABLE 3. SUBCARRIER WINDOW SELECTION

Subcarrier Window	R150 Value	Subcarrier Window	R150 Value
± 40 degrees	47K	± 20 degrees	15K
± 35 degrees	36K	± 15 degrees	10K
± 30 degrees	27K	± 10 degrees	6.2K
± 25 degrees	20K		

7. Internal/external reference indicator light modification. The module is factory configured to indicate when the processor is externally referenced, by lighting external reference LED DS5. If DS5 is to light when internally referenced, a jumper must be installed between K and L.

8. Horizontal phase nonsynchronous acceptance time frame is factory set by potentiometer R78 to 400 nanoseconds. This time value may be set between ±100 nanoseconds and ±500 nanoseconds. See Step 9 of the External Reference Adjustments for details.

9. (PAL Only) If BURST ALWAYS is jumpered on the Sync Generator, then a jumper between M and 0 is removed and M and N is jumpered and 0 and P is jumpered.

FUNCTIONAL DESCRIPTION Refer to Figure 1.

The External Reference Module has three modes of operation:

Internal - The Processor's sync and subcarrier are derived from the sync and subcarrier of the input video.

External - The Processor's sync and subcarrier are derived from externally-applied sync and subcarrier.

Auto - The video processor automatically switches between the internal and external modes of operation, depending on whether the relative timing of the input video with respect to externally-derived timing signals is within a prescribed synchronous frame, and whether a video signal is present. In determining synchronousness, three tests are involved: Horizontal phase, vertical phase, and subcarrier phase. If any of these tests fail the processor switches to the internal mode (one or more of these tests can be deleted by opening jumpers, as indicated under Operating Mode Selections). Loss of a signal constitutes a nonsynchronous condition. During monochrome processing absence of the subcarrier has no effect.

If, while in the Auto mode, no video signal is present, the processor switches to (or remains in) the external operating mode.

Video Presence Detector

The Video Presence Detector locks the processor to the external source when the video input to the processor is lost.

Horizontal Nonsynchronous Detector

The Horizontal Nonsynchronous Detector compares the timing of the H- signal from the Sync Generator Module with the timing of internal sync (regenerated from video at the Input Module) or external sync, depending on whether the processor is locked to external sync or internal sync. When the timing of the internal and external sync is within a certain time frame (adjustable from ±100 nanoseconds to ±500 nanoseconds), the Horizontal Nonsynchronous Detector sets electronic switches on the External Reference Module and the Sync Generator Module which cause the Sync Generator to lock to external sync. In this mode, the Horizontal Nonsynchronous Detector compares the timing of the internal sync and H-. H- is then synchronous with the external sync. When the timing difference between internal sync and external sync is outside the time frame, the electronic switches are activated to lock the Sync Generator to internal sync, and the Horizontal Nonsynchronous Detector compares the timing of the external sync and H-; H- in this case is synchronous with internal sync.

Vertical Nonsynchronous Detector

The Vertical Nonsynchronous Detector detects a 1/2-line timing difference (error) between the internal and external syncs. (The Horizontal Nonsynchronous Detector will not detect this noncoinci dence.) When a timing error of 1/2 line or more occurs, the Vertical Nonsynchronous Detector activates switches which lock the processor to the internal sources.

Subcarrier Phase Nonsynchronous Detection

The subcarrier phase detector compares the phase of external subcarrier with the phase of internal subcarrier. If the phase difference is within presettable limits (from ±10 to ±40 degrees), the Color Lock Module is signaled to lock to external subcarrier. The outputs of the three nonsynchronous detectors are ORed to one input of a comparator, the output of which is used to signal the Sync Generator Module, activate the electronic switches on the External Reference Module and the integrator in the subcarrier phase-locked loop of the Color Lock Module, and drive the non-sync indicator LED.

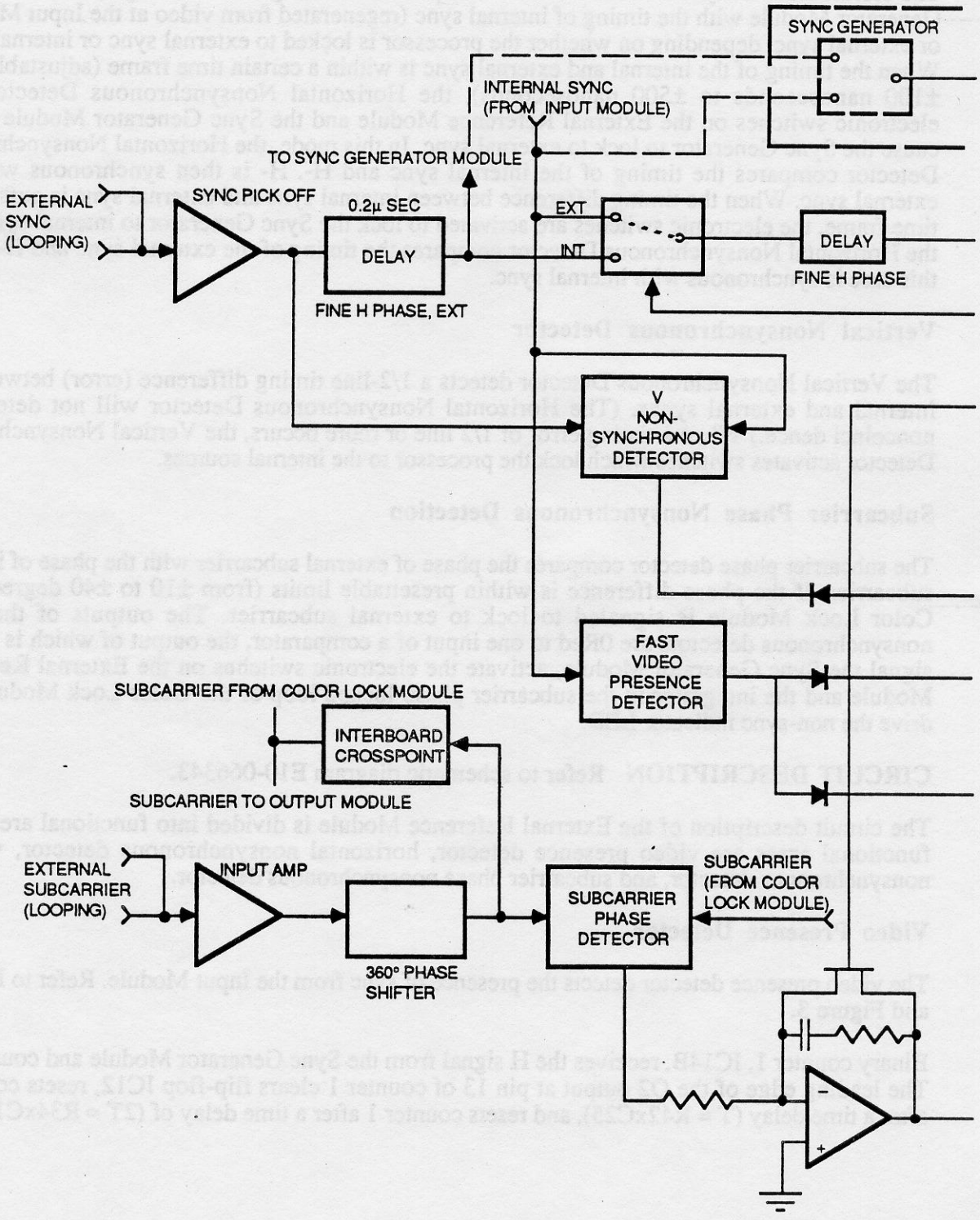
CIRCUIT DESCRIPTION Refer to schematic diagram E10-066343.

The circuit description of the External Reference Module is divided into functional areas. The functional areas are video presence detector, horizontal nonsynchronous detector, vertical nonsynchronous detector, and subcarrier phase nonsynchronous detector.

Video Presence Detector

The video presence detector detects the presence of sync from the Input Module. Refer to Figure 2 and Figure 3.

Binary counter 1, IC14B, receives the H signal from the Sync Generator Module and counts to 4. The leading edge of the Q2 output at pin 13 of counter 1 clears flip-flop IC12, resets counter 2 after a time delay (T = R42xC25), and resets counter 1 after a time delay of (2T = R34xC16).


SYNC GENERATOR
INTERNAL SYNC
(FROM INPUT MODULE)
TO SYNC GENERATOR MODULE
EXTERNAL
SYNC
(LOOPING)
SYNC PICK OFF
0.2µ SEC
DELAY
FINE H PHASE, EXT
EXT
INT
DELAY
FINE H PHASE
V
NON-
SYNCHRONOUS
DETECTOR
FAST
VIDEO
PRESENCE
DETECTOR
SUBCARRIER FROM COLOR LOCK MODULE
INTERBOARD
CROSSPOINT
SUBCARRIER TO OUTPUT MODULE
EXTERNAL
SUBCARRIER
(LOOPING)
INPUT AMP
360° PHASE
SHIFTER
SUBCARRIER
PHASE
DETECTOR
SUBCARRIER
(FROM COLOR
LOCK MODULE)

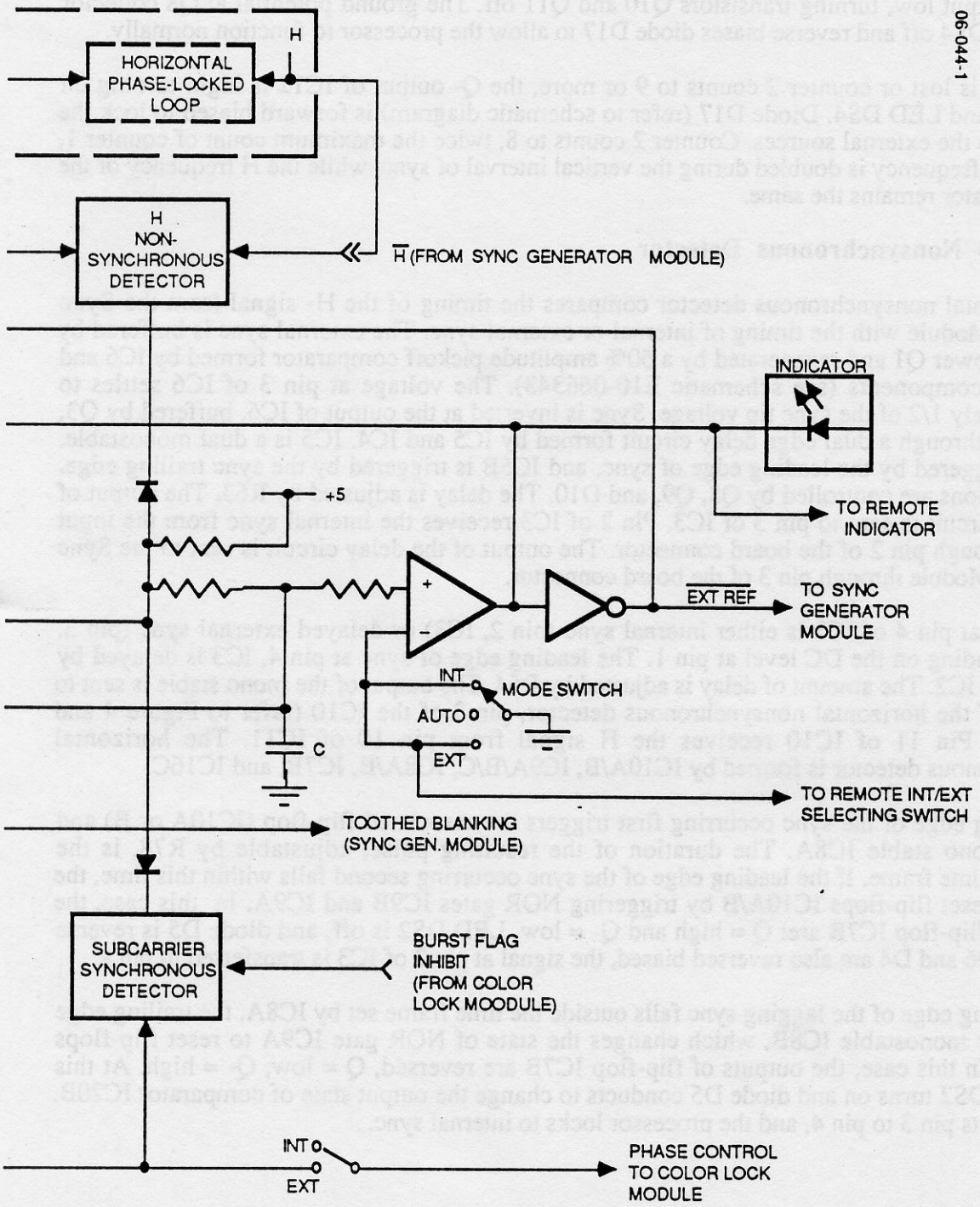


Figure 1. External Reference Module Functional Diagram

If sync is present, and counter 2 counts only to 4, the Q1 output remains low (OV) and the output of AND gate IC13B stays low holding a high at IC13C pin 13. Input pin 12 IC13C (Q0 x Q1 + Q2 + Q3) is high when the positive-going edge of IC14A's Q2 output occurs. This maintains the IC12 Q- output low, turning transistors Q10 and Q11 off. The ground potential at Q8 collector holds LED DS4 off and reverse biases diode D17 to allow the processor to function normally.

When sync is lost or counter 2 counts to 9 or more, the Q- output of IC12 is high, turning on Q11, Q10, and LED DS4. Diode D17 (refer to schematic diagram) is forward biased to lock the processor to the external sources. Counter 2 counts to 8, twice the maximum count of counter 1, because the frequency is doubled during the vertical interval of sync, while the H frequency of the Sync Generator remains the same.

Horizontal Nonsynchronous Detector

The horizontal nonsynchronous detector compares the timing of the H- signal from the Sync Generator Module with the timing of internal or external sync. The external sync is buffered by emitter follower Q1 and regenerated by a 50% amplitude pickoff comparator formed by IC6 and associated components (see schematic E10-066343). The voltage at pin 3 of IC6 settles to approximately 1/2 of the sync tip voltage. Sync is inverted at the output of IC6, buffered by Q3, and routed through a dual edge delay circuit formed by IC5 and IC4. IC5 is a dual monostable. IC5A is triggered by the leading edge of sync, and IC5B is triggered by the sync trailing edge. Their durations are controlled by Q8, Q9, and D10. The delay is adjusted by R63. The output of the delay circuit is sent to pin 3 of IC3. Pin 2 of IC3 receives the internal sync from the input module through pin 2 of the board connector. The output of the delay circuit is sent to the Sync Generator Module through pin 3 of the board connector.

The signal at pin 4 of IC3 is either internal sync (pin 2, IC3) or delayed external sync (pin 3, IC3), depending on the DC level at pin 1. The leading edge of sync at pin 4, IC3 is delayed by monostable IC2. The amount of delay is adjusted by R64. The output of the mono stable is sent to one port of the horizontal nonsynchronous detector, pin 3 of the IC10 (refer to Figure 4 and Figure 5). Pin 11 of IC10 receives the H signal from pin 10 of IC11. The horizontal nonsynchronous detector is formed by IC10A/B, IC9A/B/C, IC8A/B, IC7B, and IC16C.

The leading edge of the sync occurring first triggers the associated flip-flop (IC10A or B) and triggers mono stable IC8A. The duration of the resulting pulse, adjustable by R78, is the horizontal time frame. If the leading edge of the sync occurring second falls within this time, the edge will reset flip-flops IC10A/B by triggering NOR gates IC9B and IC9A. In this case, the outputs of flip-flop IC7B are: Q = high and Q- = low. LED DS2 is off, and diode D5 is reverse biased. If D6 and D4 are also reversed biased, the signal at pin 2 of IC3 is transferred to pin 4.

If the leading edge of the lagging sync falls outside the time frame set by IC8A, the trailing edge will trigger monostable IC8B, which changes the state of NOR gate IC9A to reset flip-flops IC10A/B. In this case, the outputs of flip-flop IC7B are reversed, Q = low, Q- = high. At this time LED DS2 turns on and diode D5 conducts to change the output state of comparator IC20B. IC3 connects pin 3 to pin 4, and the processor locks to internal sync.

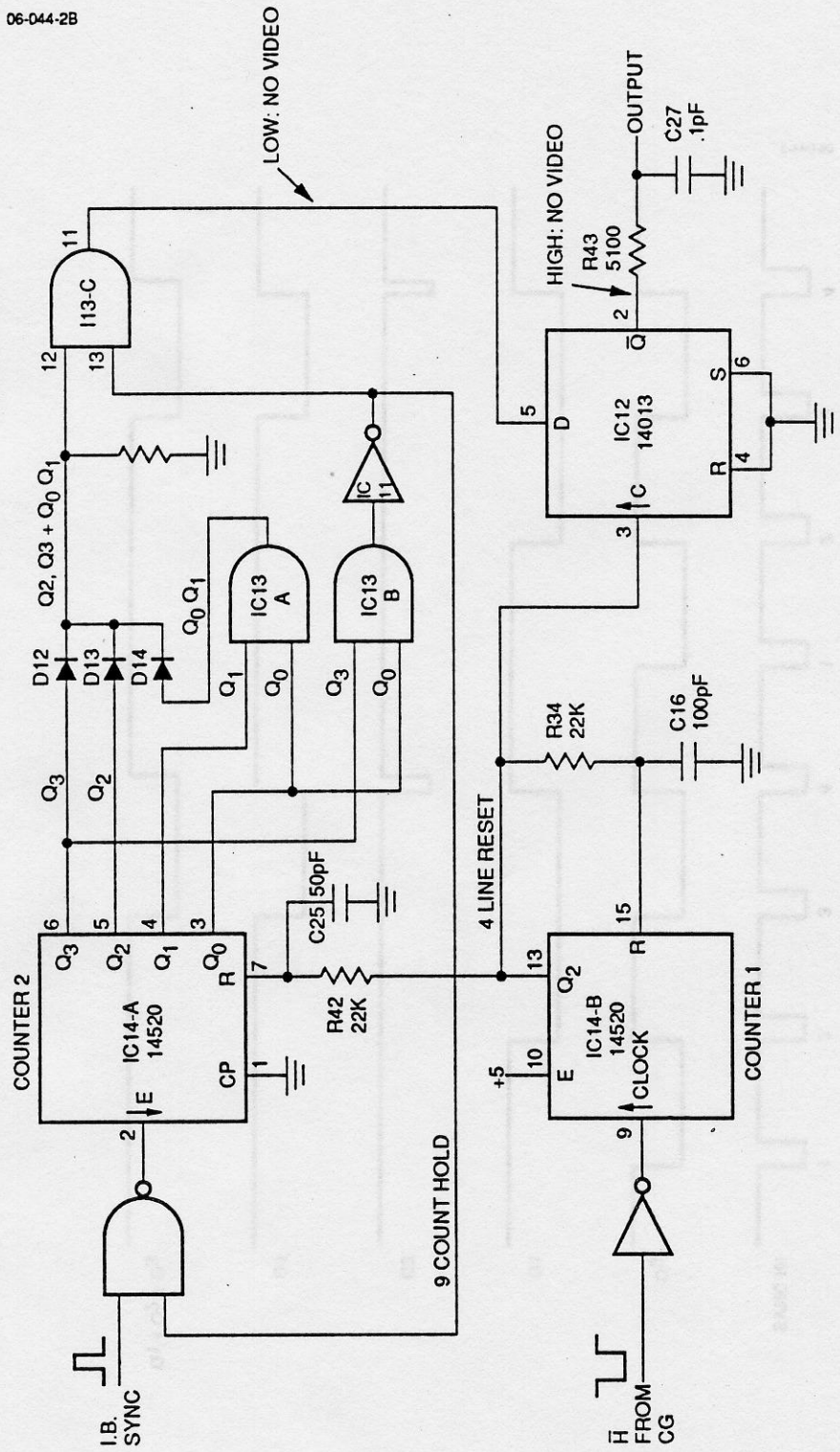


Figure 2. Video Presence Detector, Functional Diagram

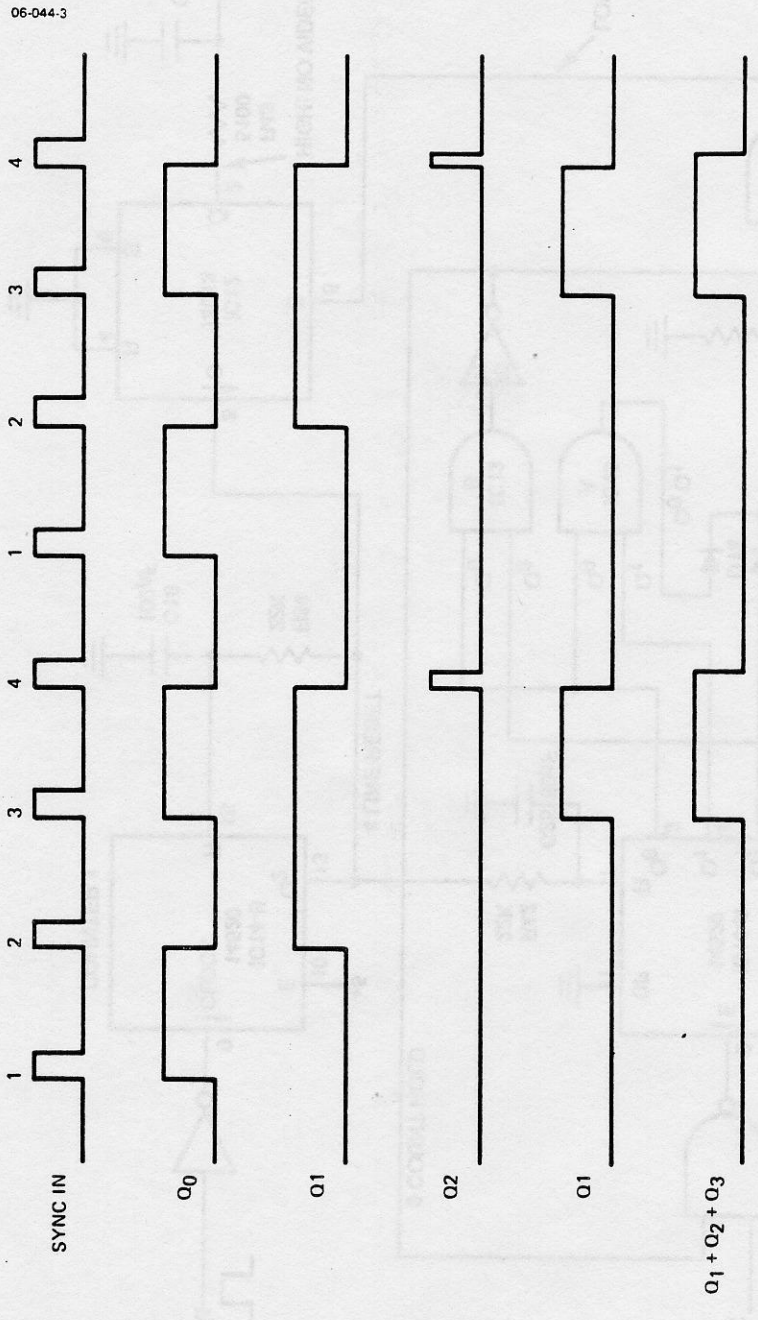


Figure 3. Video Presence Detector, Timing Diagram

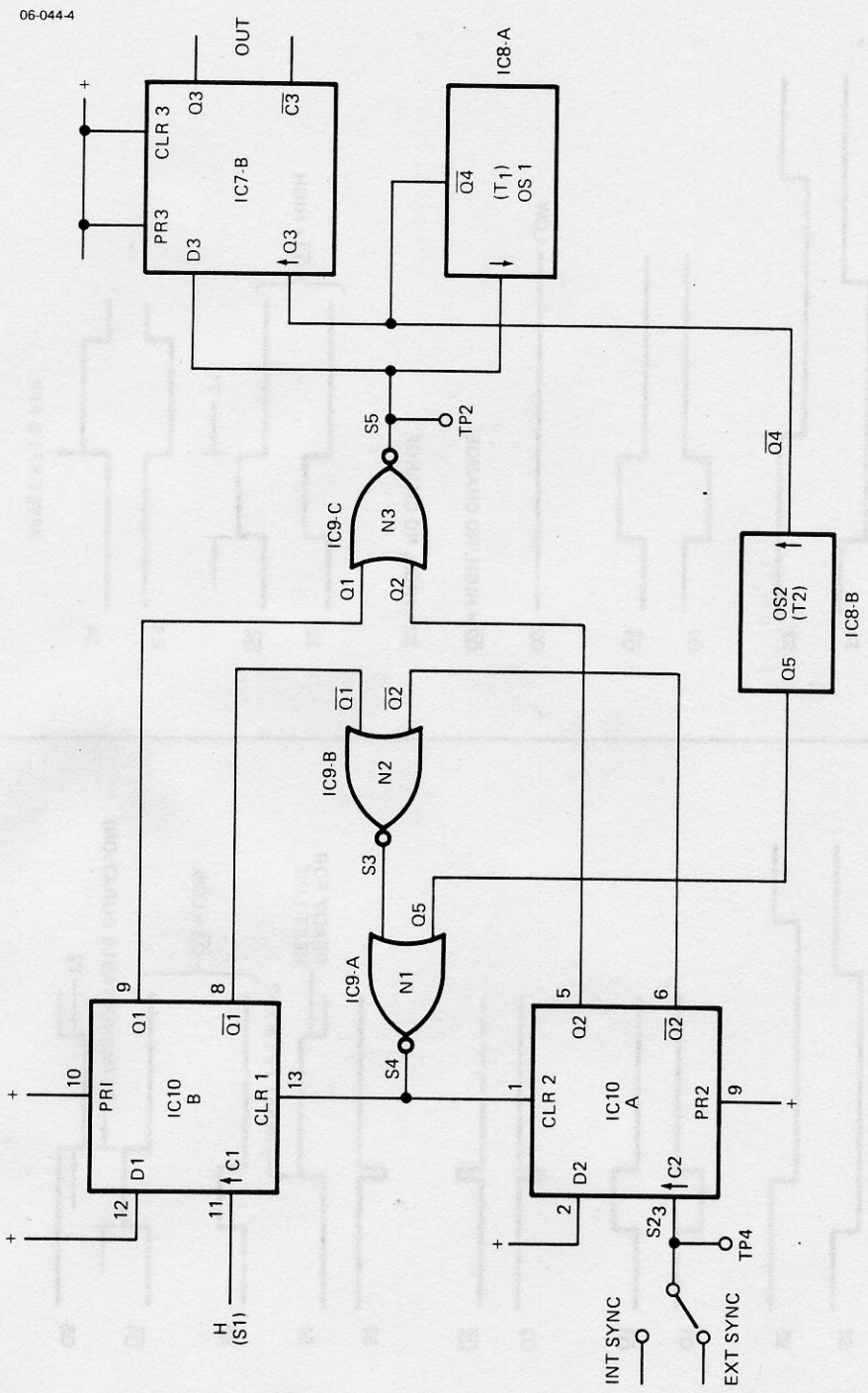


Figure 4. Horizontal Nonsynchronous Detector, Functional Diagram

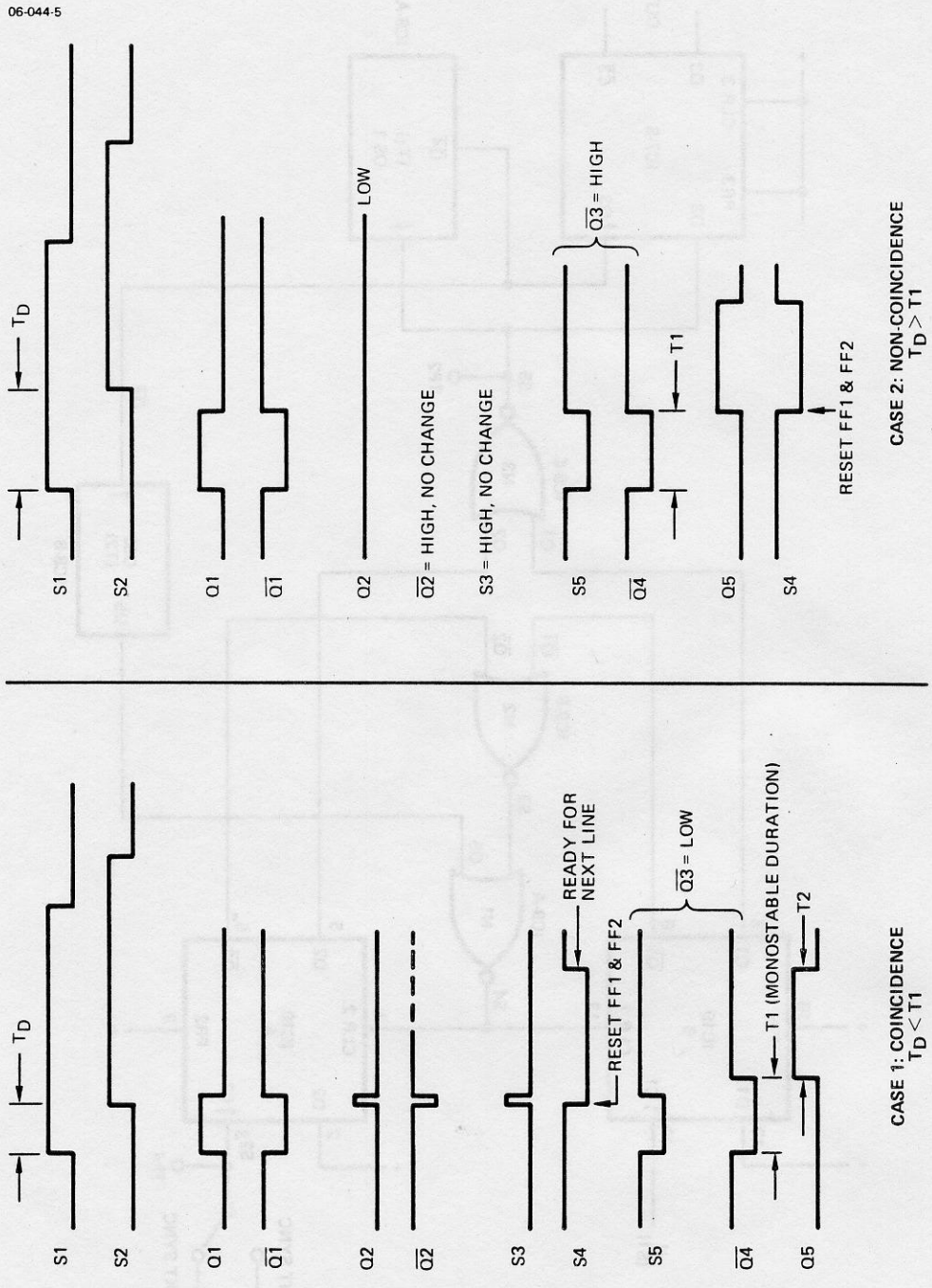


Figure 5. Horizontal Nonsynchronous Detector, Timing Diagram

Vertical Nonsynchronous Detector

The vertical nonsynchronous detector, IC16-A, the inputs of which are the external sync (pin 1) and internal sync (pin 2), has two modes of operation; synchronous and nonsynchronous (see Figure 6).

Synchronous Operation

The input signal at IC16A pin 1 is external sync and at pin 2 is in ternal sync. The output signals at pin 3 of IC16 are a train of narrow pulses corresponding to the edges of syncs. The output pulses trigger retriggerable monostable IC1A, which produces output pulses at pin 7 of approximately 10 microseconds duration. When the positive-going trailing edge of the 10 microsecond pulse occurs, the level at pin 12 of flip-flop IC7A is low so that the state of flip-flop IC7-A remains unchanged. At this time LED DS1 is off, diode D4 is reversed biased, and the processor is locked to the external sync sources.

Nonsynchronous Operation

If the internal sync is displaced by 1/2 line relative to the external sync (field 1 of the internal sync coincides with field 2 of the external sync), the horizontal nonsynchronous detector cannot detect the nonsynchronism. The exclusive OR gate, IC16A, detects the difference in the vertical interval and triggers flip-flop IC7A, the output pulse of which triggers monostable IC1B. The duration of IC1B's pulse is approximately 22 milliseconds, which is longer than a field. During this condition LED DS1 is turned ON to indicate the vertical nonsynchronism, D4 is forward-biased, and the processor is forced to lock internally.

Subcarrier Phase Nonsynchronous Detector

The subcarrier phase nonsynchronous detector circuit consists of an input amplifier, a phase shifter, phase detectors, and an inter-board subcarrier crosspoint. The external subcarrier is connected to the subcarrier input amplifier through pin 33 of the module connector. The signal is amplified 6dB by input amplifier Q34, Q36, complementary pair Q35, Q31, and current sources Q33 and Q36. Diode D11 sets the emitter bias current for complementary pair Q35 and Q31. From the input amplifier, the signal is routed through a five-step delay line (DL1) and switch (S1) which function as a step phase control. The signal is buffered by Q28 and phase-shifted by the all-pass network formed by C34, R151, R91, R90, and R119. This signal is then applied to two phase detectors, IC19, and IC17, and the inter-board subcarrier crosspoint. The other input to phase detector IC19 is the internal subcarrier from the Color Lock Module. The differential output voltage of IC19 is directly proportional to the phase difference of the two subcarriers. This voltage is amplified by operational amplifier IC18A, and averaged by integrator IC20A.

When the DC voltage output of integrator IC20A, pin 1, is within the window set by R141, R150, and R131, the levels at pins 8 and 14 of IC20 are high, and diodes D23 and D24 are reverse-biased. Diode D6 is also reverse-biased, permitting the processor to be locked externally; FET's Q4 and Q5 are off, and FET Q6 is on to close the phase-locked loop.

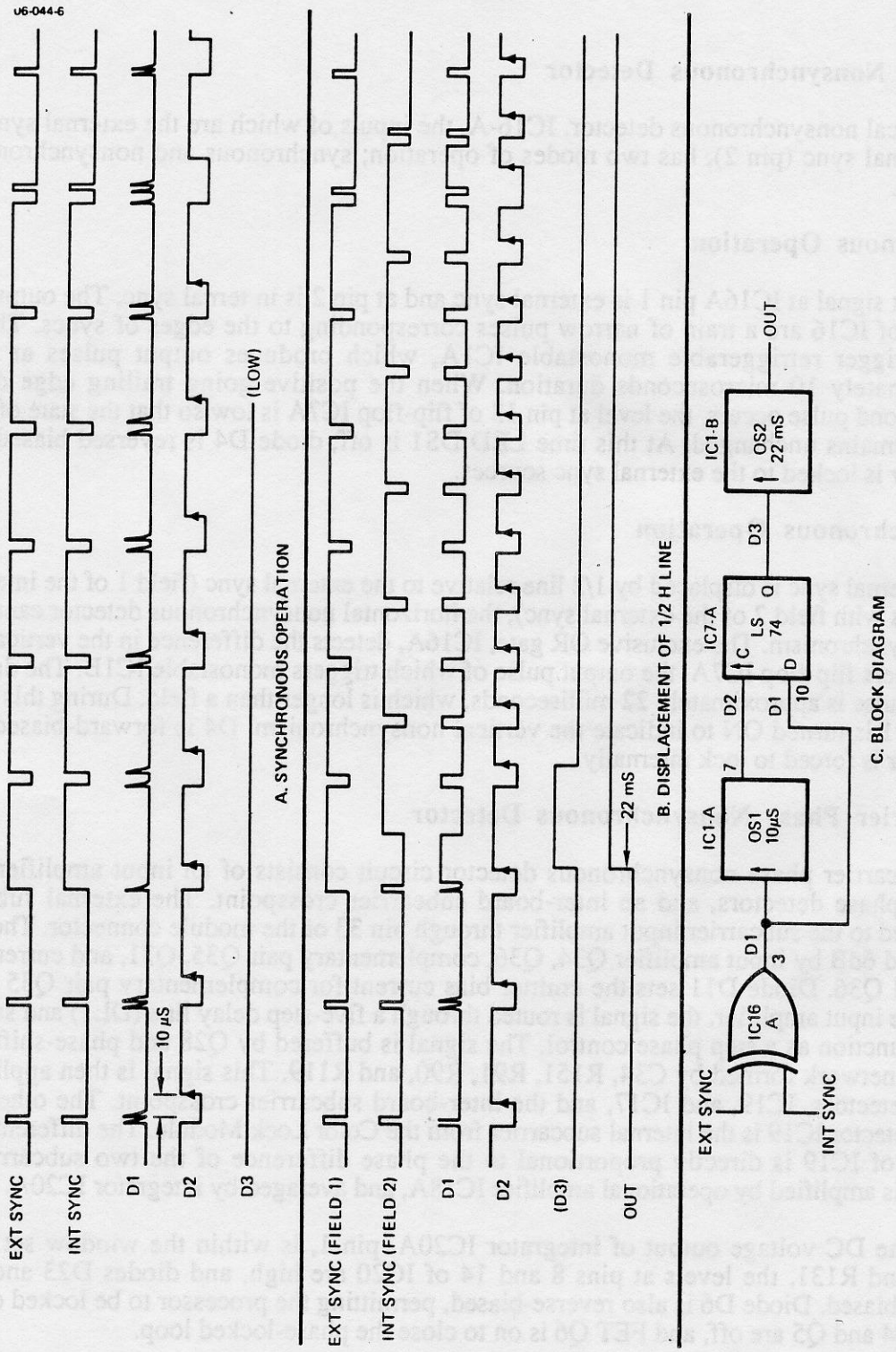


Figure 6. Vertical Nonsynchronous Detector, Timing Diagram

If the integrator output, IC20A, pin 1, is outside the window limits, diode D23 or D24 will ground one input of NOR gate IC9D, and LED DS3 will turn on to indicate that the external subcarrier phase is out of lock range, and the nonsync output at pin 25 signals the processor to lock internally. During this condition FETs Q4 and Q5 are turned on by Q7, and Q6 is held off by IC20B. When Q4 is turned on it provides hysteresis for the integrator. Turning Q5 on and turning Q6 off opens the processor's phase-locked loop.

The second phase detector, IC17, which shares the same external sub carrier input with IC19, receives the internal subcarrier after it has been delayed 90 degrees by network L1, C29, and C30. The output of IC17 is amplified by IC18B and 0Red by diode D22 to the anode node of D23 and D24. This interrupts the functioning of the phase-locked loop when the subcarrier phases are approximately 180 degrees apart. This prevents positive feedback from occurring when the external subcarrier is out of phase with the color lock subcarrier.

Inter-Board Crosspoint

In the external reference mode, the subcarrier from the Color Lock Module must be turned off and routed to the Output Module. This is accomplished by an inter-board crosspoint. The coax which runs from J1-35, J2-44 and J4-27 routes this signal. When in the internal mode or when no External Reference Module is used, the dc voltage on this coax is high, forward-biasing a diode on the Color Lock Module, and sending the subcarrier directly to the Output Module. When the External Reference Module is inserted and Q39 is conducting, the dc voltage is high and Q26is on, which reverse-biases the base-to-emitter junction of Q27 and PIN diode D26. Q25 acts as a shunt switch. When in the external mode, external subcarrier is phase-shifted by the tapped delay line and the all-pass filter. Q29 and Q30 form a differential amplifier pickoff for the all-pass filter. Delay line C37, C38, and L3 control system burst phase to match in the internal and external modes, and emitter follower Q27 drives the inter-board crosspoint.

When pins S and T are jumpered together, diode D15 holds the Burst Flag Inhibit line (pc module pin 6) low. It also holds the Inter-board Crosspoint on. This causes regenerated burst (referenced to external subcarrier) to always appear on the output video of the 3240/3241, regardless of whether burst is present on the input video. This feature operates only when the processor is in the external reference mode.

±10 Volt Regulator Refer to schematic diagram C10-058030.

The ±10 volt regulator for the 3400/3200 Series modules receives ±12 to ±18 volts unregulated DC from the 3200A Power Supply and provides regulated ±10 volts to the module. The incoming positive dc voltage is decoupled by L500 and C500. Further decoupling and current limiting is provided by C501 and RN501R. At startup the regulator output is at zero, and series pass transistor Q502 is held off by RN501S. During startup, current flows through R500, RN501T, and R502, resulting in a small positive dc voltage at the output. This voltage is applied to the inverting input of IC500A through RN501K and RN501L. Network RN501N, R504, and RN501H divides this voltage in half and applies it to the noninverting input of IC500A. The resulting input imbalance causes the output of IC500A to swing negative. The voltage developed across RN501P causes current to flow in Q503 and Q502. When Q502 is conducting, the output of the regulator rises until the voltage at the wiper arm of R504 is equal to the breakdown voltage of Q506 (6.45V, ±4%). At this point the IC inputs are balanced, and the loop stabilizes.

Operation of the negative regulator is similar to that of the positive regulator, except IC500B is referenced to ground and connected to the output of the positive regulator. IC500B senses the difference between positive and negative outputs through RN501D and RN501M. During normal operation, the negative regulator tracks the positive regulator output. However, if the negative output voltage is pulled toward ground due to the current limiting of Q501, the base of Q507 goes positive. Q507 then starts to conduct, reducing the reference to the positive regulator. The positive regulator then tracks the negative regulator output during overload conditions.

The regulator comes in two versions. The first version, intended to supply less than 100 milliamperes, has 4.7 ohm resistors for R500 and R501 and uses an MPSU51 transistor for Q502 and an MPSU01 for Q50. The second version supplies more than 100 milliamperes, and uses 2.7 ohm resistors for R500 and R501, and an MJE371 and MJE521 for Q502 and Q505, respectively.

ADJUSTMENTS

NOTE

Under normal operating conditions, the External Reference Module requires no adjustments. The following adjustment procedures should NOT be completed unless repairs affecting the setting of adjustments have been made.

Test Equipment Required

Video test signal generator	Tek 1410 or equivalent
Vectorscope	Tek 520 or equivalent
Oscilloscope	Tek 465 or equivalent
3200 extender	066301-01
Digital voltmeter	---------
Calibrated attenuator	---------

One 2RU 3240 or 3241 processor frame* (NTSC 093683, PAL and PAL-M 096309) plus: Input Module, Output Module, Color Lock Module, and Sync Generator Module.
*Two processors are required to check the function of the vertical nonsynchronous detector.

ALIGNMENT PROCEDURE

Initial Conditions

1. Adjust the video processor system as outlined in the instruction manual. Turn off the SC-H subcarrier switch on the Sync Generator Module (NTSC only) before aligning the External Reference or a switchable delay line.

2. Verify that pins A-B, C-D, and E-F on the External Reference Module ARE jumpered.

3. Place the External Reference Module on an extender card.

4. Verify that pins S and T on the External Reference Module ARE NOT jumpered.

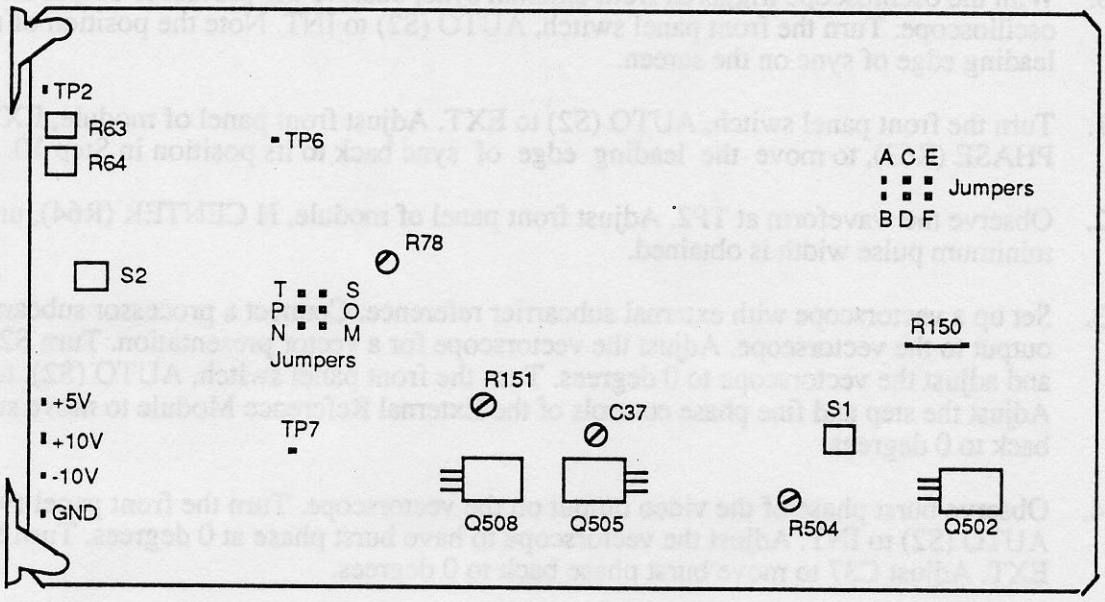


Figure 7. External Reference Module Component Location

Voltage Regulator Adjustments

1. Connect the DVM to the +10V test point and ground. Adjust R504 for a reading of +10.0V.

2. Check the -10V test point. The voltage should be -10.0V, ±0.2V.

3. Connect the collector of Q502 to ground with a 10 ohm jumper. Do not hold the resistor body with your fingers.

4. Check the + and - 10V outputs with the DVM. They should be within 1.2V of ground.

5. Remove the jumper from Q502 and connect it between the collector of Q505 and ground.

6. Using the DVM, check the positive and negative 10V outputs. The negative output should be approximately -1V, and the positive should be approximately +2.3V.

7. Remove the jumper from Q505 and connect between the collector of Q508 and ground. Check the voltage at +5V test point. It should drop to less than +2.5V. Remove the jumper from Q508. This step concludes the adjustments of the voltage regulator.

External Reference Adjustments

8. Connect the ramp signal to the processor input. Connect the composite sync and subcarrier from the signal generator to J12 and J14 of the processor. Terminate those inputs with 75Ω.

9. Turn the front panel switch, AUTO (S2), to EXT. Watch the waveform at TP6 on the oscilloscope, which is triggered by external composite sync from the test signal generator. Adjust R78.The pulse width should be variable from 100 nanoseconds to 500 nanoseconds. Set the pulse width at 400 nanoseconds.

10. With the oscilloscope triggered from external sync, observe the processor output on the oscilloscope. Turn the front panel switch, AUTO (S2) to INT. Note the position of the leading edge of sync on the screen.

11. Turn the front panel switch, AUTO (S2) to EXT. Adjust front panel of module, EXT H PHASE (R63), to move the leading edge of sync back to its position in Step 10.

12. Observe the waveform at TP2. Adjust front panel of module, H CENTER (R64), until a minimum pulse width is obtained.

13. Set up a vectorscope with external subcarrier reference. Connect a processor subcarrier output to the vectorscope. Adjust the vectorscope for a vector presentation. Turn S2 to INT and adjust the vectorscope to 0 degrees. Turn the front panel switch, AUTO (S2) to EXT. Adjust the step and fine phase controls of the External Reference Module to move subcarrier back to 0 degrees.

14. Observe burst phase of the video output on the vectorscope. Turn the front panel switch, AUTO (S2) to INT. Adjust the vectorscope to have burst phase at 0 degrees. Turn S2 to EXT. Adjust C37 to move burst phase back to 0 degrees.

15. Set front panel switch AUTO (S2) to AUTO. All LED's should be OFF (except for EXT REF, DS5).

LED Test Adjustments

16. Remove the video input from the processor. VIDEO PRESence LED DS4 on front panel and EXTernal REFerence LED DS5 should be ON. Reconnect the video input to the processor.

17. Adjust FINE Ø control to move burst phase toward +15 degrees limit*. When it reaches this limit, it should fall back to 0 degrees, and SUBRANGE (DS3) should turn ON, EXT REF (DS5) OFF. Readjust the FINE Ø control (R151) to place the burst phase at 0 degrees with SUBRANGE (DS3) OFF and EXT REF (DS5) ON.

18. Observe the leading edge of sync on the oscilloscope. Adjust the oscilloscope to have this edge at 0 nanoseconds (middle of the screen). Adjust front panel control EXT H PHASE (R63), fully clockwise then fully counterclockwise. The leading edge of sync should move within the limits of from -400 nanoseconds to +400 nanoseconds. When it reaches either limit, it should fall back to 0 nanoseconds, and LED's H NON-SYNC (DS2) should turn ON, EXT REF (DS5) OFF. Readjust EXT H PHASE (R63) to its initial position.

19. This test requires a second video processor with four basic modules: the Input Module, Output Module, Sync Generator Module, and the Color Lock Module. Remove the video input from the first processor and apply it to the second one. Connect the video output of the second processor to the input of the first one. (On the Sync Pulse Generator module, turn front panel switch VERT PHASE (S3) to ADVANCE position.) Notice that LED V NON-SYNC (DS1) should turn ON and EXT REF (DS5) OFF.

*15 degrees if R150 equals 10K ohms (see schematic table)

A1	PILOT RUN-REL.				

PICK-OFF

DUAL EDGE DELAY

VIDEO PRESENCE DETECTOR

FINE-H Ø

VERTICAL NON-SYNCHRONISM DETECTOR

HORIZONTAL NON-SYNCHRONISM DETECTOR

SUBCARRIER CROSSPOINT

SUBCARRIER INPUT AMPLIFIER

PHASE SHIFTER

+5V REGULATOR

SUBCARRIER HYSTERESIS

LED DRIVER (4 PL)

EXT SYNC INPUT

SYNC (FROM INPUT BOARD)

R FROM SG

COLOR LOCK SUB

EXT SUB

SC INTERBOARD CROSSPOINT

BURST FLAG INHIBIT

+16V UNREG

-16V UNREG

GND

POWER SUPPLY REF DWG NO. C10-058030-02

EXT SYNC O TO S.G.

TOOTHED BLANKING (SYNC GEN, OUTPUT)

RM EXT REF INDICATOR

TO EXT REF SYNC GEN

NONSYNC OUTPUT

TO PAL COLOR LOCK

TO COLOR LOCK

EXT REF TO PAL SYNC GEN

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS 1/4 W, 5%. VALUES ARE IN OHMS(Ω).
   ALL CAPACITORS ARE IN MICROFARADS.
   ALL DIODES ARE 1N4148
   *DENOTES PAL ONLY
   **PAL & PAL-M ONLY.
   ↻ DENOTES CLOCKWISE ROTATION
   (B)-DENOTES CONNECTOR PIN AND NUMBER
   LAST COMPONENT IDENT. NO. USED

2. SUBCARRIER WINDOW (R87)

± 40°	47K	RESISTOR VALUE
± 35°	36K	CORRESPONDS TO
± 30°	27K	SC-SYNCHRONISM
± 25°	20K	WINDOW.
± 20°	15K	
± 15°	10K	
± 10°	6.2K	

3.

LED DRIVER	Qx	Qy	Rx	Ry	Rz
4	Q15	Q14	R49	R53	R54
1	Q20	Q21	R47	R59	R60
2	Q19	Q18	R46	R57	R58
3	Q16	Q17	R48	R55	R56

4. NORMAL - JUMPER M TO O
   FOR ALWAYS BURST PAL - JUMPER M TO N
   JUMPER O TO P

5. FOR BURST ALWAYS NTSC - JUMPER S-T, OPEN A-B

MODULAR PRODUCTS

STS

SCHEMATIC DIAGRAM, EXTERNAL REFERENCE

10-066343-02/12 AT

NONE

12-8-83